

ESREF 2026

TU WIEN

iμe INSTITUTE FOR MICROELECTRONICS

EUROPEAN SYMPOSIUM ON
RELIABILITY OF ELECTRON DEVICES,
FAILURE PHYSICS AND ANALYSIS
SEPTEMBER 21-24, 2026

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TECHNICAL PROGRAM

2026 VIENNA ESREF

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Welcome to ESREF 2026

We are delighted to welcome you to the **37th edition of ESREF**, hosted in the historic and culturally rich city of **Vienna**, Austria, by the **Institute for Microelectronics at TU Wien**. As a city renowned for its long-standing contributions to science, engineering, and innovation, Vienna provides an inspiring setting for this international symposium, bringing together leading experts in reliability, failure analysis, and semiconductor technology from around the world.

Over the decades, **ESREF** has established itself as one of the premier international forums for the exchange of cutting-edge research, innovative ideas, and technological advancements in the field of micro- and nanoelectronics reliability. The technical program spans **ten specialized tracks**, covering a broad spectrum of timely and important topics, including reliability assessment, nanoelectronics reliability, advances in failure analysis, power device reliability, photonics, MEMS and sensors, packaging and assembly, as well as electronics designed for extreme environments.

This year's program is the result of an extraordinary community effort. The Organizing Committee and the Technical Program Committee have worked over many months to assemble an exciting and comprehensive technical program that reflects the latest developments in our field. We are particularly proud to present around **30 invited presentations**, including inspiring keynote lectures, in-depth tutorials, and specialized short courses delivered by internationally recognized experts.

The response from the reliability community has been truly remarkable. We received **more than 250 abstract submissions** from around the world, demonstrating the continued vitality and relevance of **ESREF**. The paper

Welcome to ESREF 2026

selection process involved **nearly 300 reviewers**, whose dedication, expertise, and careful evaluations ensured that the highest-quality scientific contributions were selected for presentation.

Finally, we would like to express our sincere gratitude to all authors, reviewers, session organizers, track chairs, invited speakers, exhibitors, sponsors, and volunteers whose commitment has made **ESREF 2026** possible. It is a great honor for TU Wien to host this year's symposium, and we are proud to welcome the international reliability community to Vienna. We wish you an inspiring conference, productive discussions, and an enjoyable stay in one of Europe's most beautiful and vibrant cities.

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Recognized Green Event

EcoEvent
Environment is VIP in Vienna

ESREF 2026 in Vienna has been officially recognized as a **Green Event** under the city's "EcoEvent" guidelines, proving that world-class science is strongly committed to sustainability.

Our Green Commitments:

- Low-waste catering – seasonal, regional, and vegetarian-friendly menu options.
- Eco-friendly materials – no single-use plastics, reusable or compostable products only.
- Travel awareness – encouraging public transport, rail, and shared mobility where possible, with options to offset unavoidable flights.
- Digital-first – reduced printing, paperless proceedings, and electronic signage.
- Sustainable printing – printed materials will use environmentally friendly, certified paper.

Why does this matter for semiconductor research?

The semiconductor industry is accelerating its decarbonization efforts by expanding renewable energy sourcing and improving operational efficiency, while addressing challenges such as local grid limitations and other sustainability hurdles. By making **ESREF 2026** a **Green Event**, we show that scientific excellence and sustainability are not just compatible, but are mutually reinforcing. Together, we are advancing technology for a better, greener future.

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Main Patron Spotlight: Infineon Technologies

Driving decarbonization and digitalization. Together

Semiconductors are crucial to solve the energy challenges of our time and shape the digital transformation. This is why **Infineon** is committed to actively driving decarbonization and digitalization. As a global semiconductor leader in power systems and IoT, we enable game-changing solutions for green and efficient energy, clean and safe mobility, as well as smart and secure IoT.

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With great pride, **Infineon also** supports ESREF 2026, underlining its commitment to advancing research, innovation, and sustainable progress in the semiconductor community.

Silver Sponsor



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Floorplan: Sections A, B, and C



Floorplan: Sections A, B, and C

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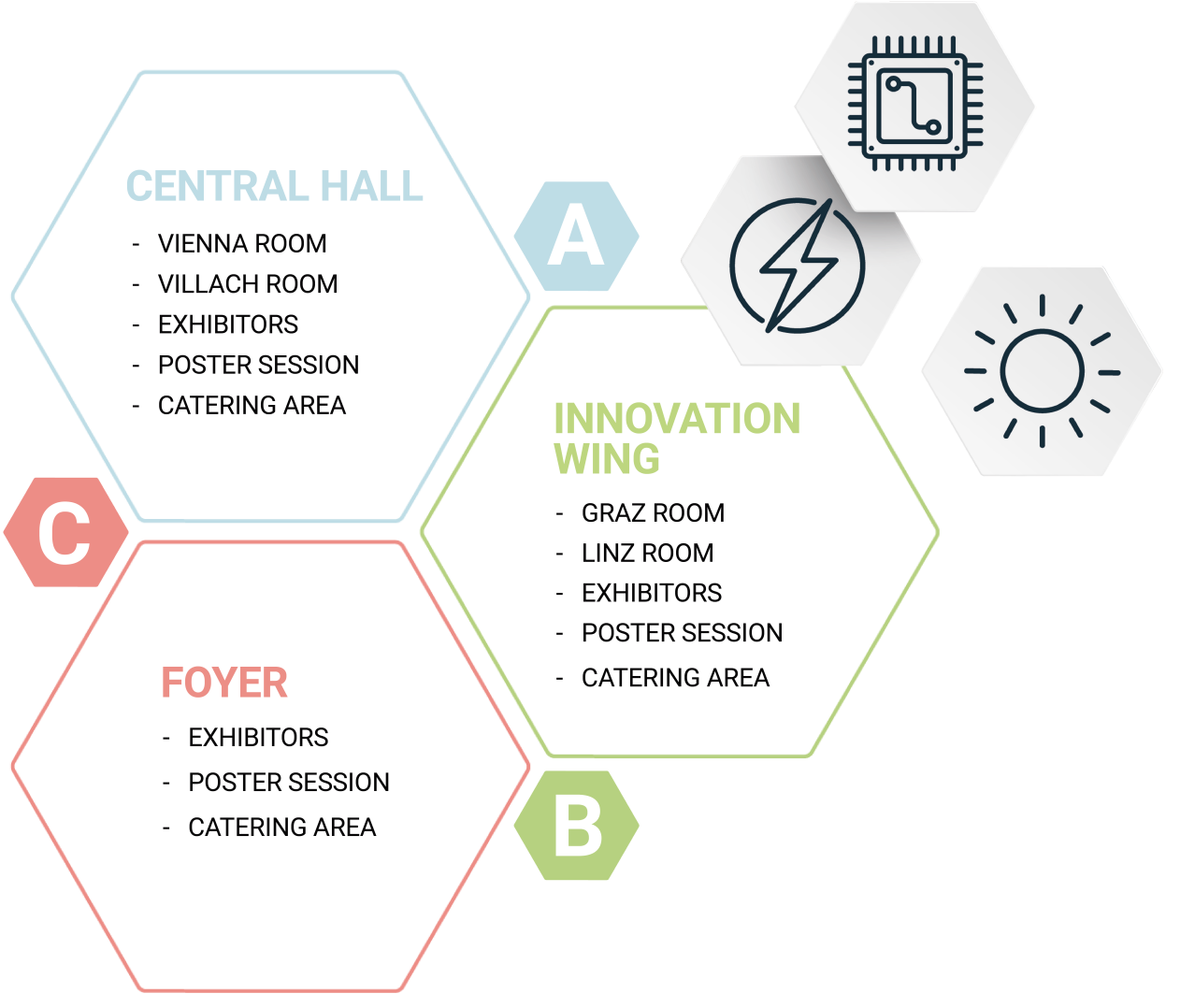
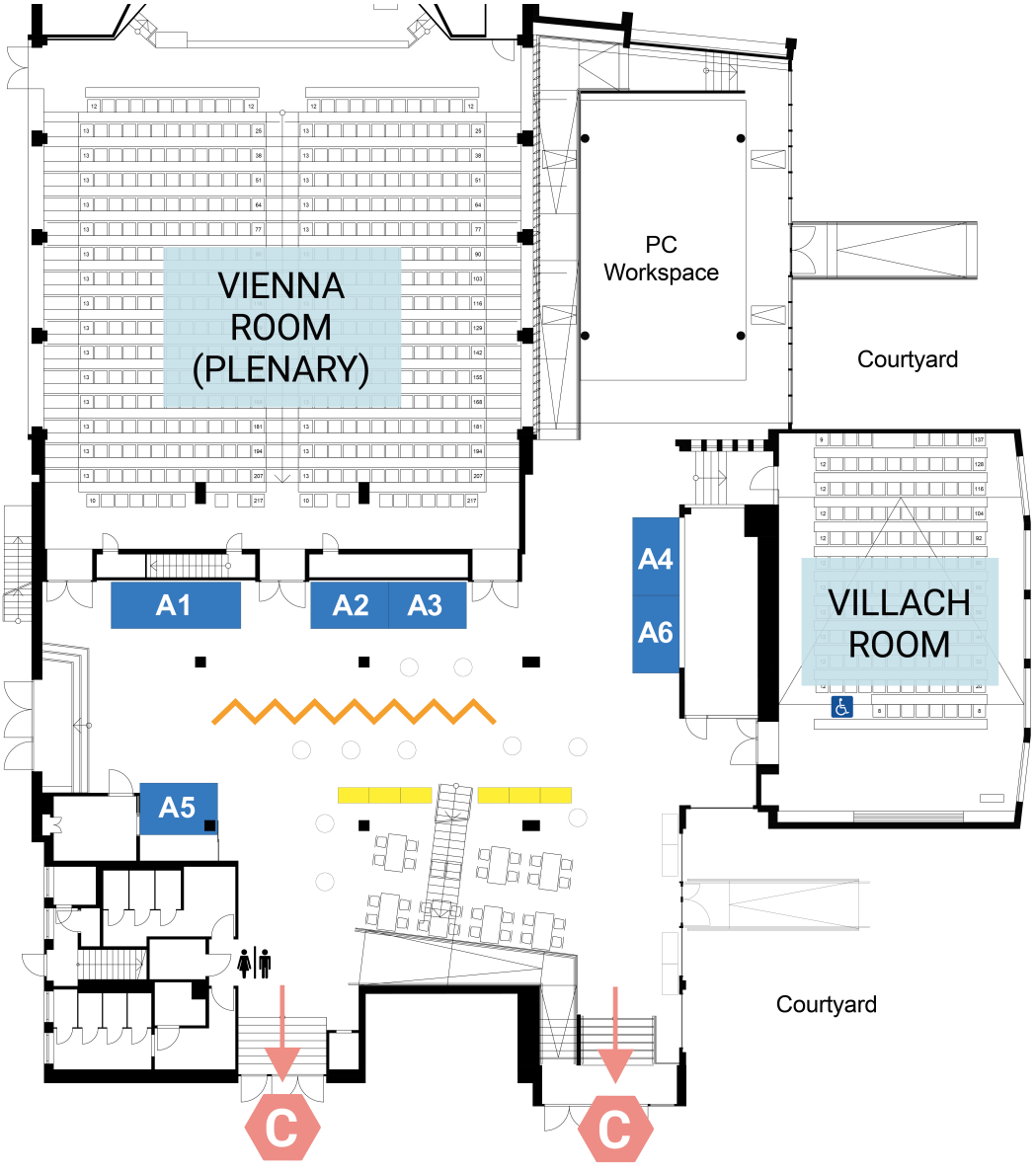


Floorplan & Exhibition

2026 VIENNA ESREF

Section A: Central Hall



Section A: Central Hall

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A1 infineon

A2 KUMMER SEMICONDUCTOR TECHNOLOGY

A3 kleindiek nanotechnik

A4 opSens Solutions

A5 eurofins | MASER

A6 IMINA TECHNOLOGIES

Floorplan & Exhibition

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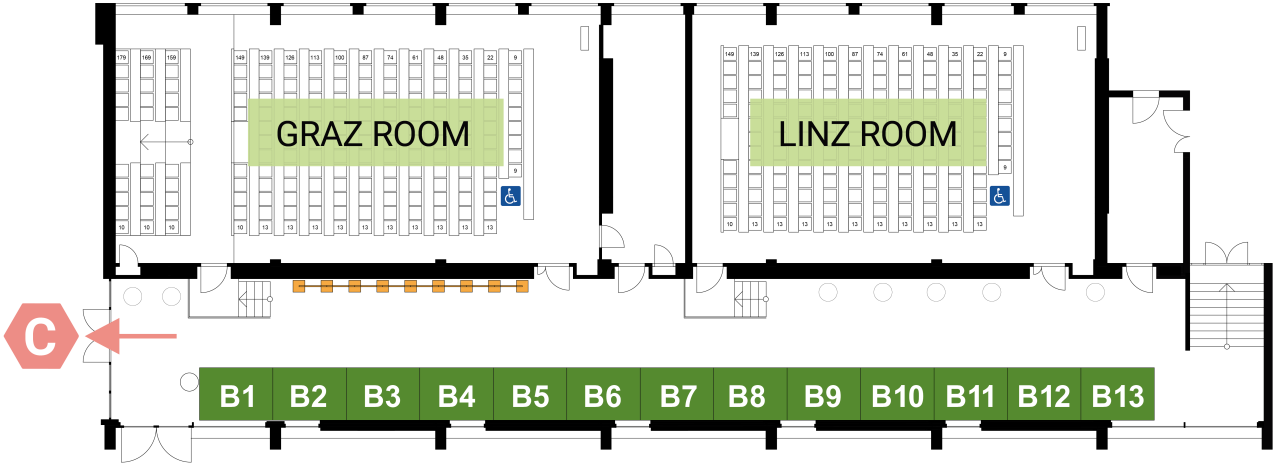
Section B: Innovation Wing

B

EXHIBITORS

POSTER SESSION



Section B: Innovation Wing

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B1 HAMAMATSU PHOTON IS OUR BUSINESS

B2 microsanJ

B3 SEIWA OPTICAL

B4 PVA TePla

B5 ZABRE

B6 FMS BONDTEC

B7 SECTOR TECHNOLOGIES

B8 MERCIA SEMICONDUCTOR

B9 HITACHI

B10 CHECKPOINT TECHNOLOGIES, LLC

B11 衡信分析科技股份有限公司 Trinity Analysis Tech., Co., Ltd TIA TRINITY ANALYSIS

B12 QUANTUM DIAMONDS SENSOR TECHNOLOGY

B13 DIGIT DC CONCEPT FA Solution and HighTech Equipment

Floorplan & Exhibition

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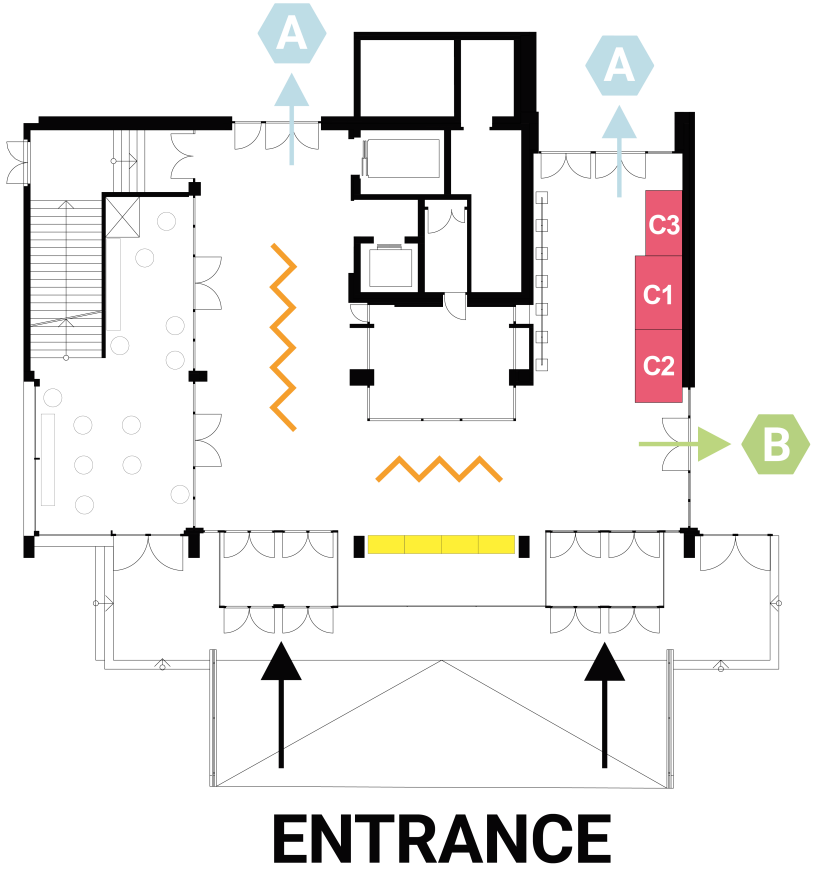
Section C: Foyer

C

EXHIBITORS

CATERING AREA

POSTER SESSION



Section C: Foyer

C1 JEOL

C2 ALLIED HIGH TECH PRODUCTS

C3 scia systems

Program Overview

2026 VIENNA ESREF

Monday, 21 September 2026

	Monday, Sept. 21st, 2026				
	Vienna Room (EI7)	Villach Room (EI8)	Graz Room (EI9)	Linz Room (EI10)	Exhibition Area
08:00 - 08:20					
08:20 - 08:40					
08:40 - 09:00					
09:00 - 09:20	Registration desk opens				Set up Exhibition Area
09:20 - 09:40					
09:40 - 10:00					
10:00 - 10:20					
10:20 - 10:40					
10:40 - 11:00					
11:00 - 11:20					
11:20 - 11:40					
11:40 - 12:00	Welcome Snack				
12:00 - 12:20					
12:20 - 12:40					
12:40 - 13:00					
13:00 - 13:20	(TUT-1) Tutorial 1 Srabanti Chowdhury		(TUT-2) Tutorial 2 Andreas Martin	(TUT-3) Tutorial 3 Hussam Amrouch	Exhibition
13:20 - 13:40					
13:40 - 14:00					
14:00 - 14:20	(TUT-4) Tutorial 4 Peter Moens	(TUT-5) Tutorial 5 Aidan Taylor	(TUT-6) Tutorial 6 Xavier Garros	(TUT-7) Tutorial 7 Joe McPherson	
14:20 - 14:40					
14:40 - 15:00					
15:00 - 15:20	Coffee break				
15:20 - 15:40					
15:40 - 16:00	(SC1) Short Course 1 Power Electronics		(SC2) Short Course 2 Emerging Technologies (IEEE EDS Webinar)		
16:00 - 16:20					
16:20 - 16:40					
16:40 - 17:00					
17:00 - 17:20					
17:20 - 17:40					
17:40 - 18:00					
18:00 - 18:20					
18:20 - 18:40					
18:40 - 19:00					
19:00 - 19:20	Welcome Reception Kuppelsaal TU Wien				
19:20 - 19:40					
19:40 - 20:00					
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21:40 - 22:00					

Tuesday, 22 September 2026

2026 VIENNA ESREF

	Tuesday, Sept. 22nd, 2026				
	Vienna Room (EI7)	Villach Room (EI8)	Graz Room (EI9)	Linz Room (EI10)	Exhibition Area
08:00 - 08:20					
08:20 - 08:40	Registration desk opens				
08:40 - 09:00					
09:00 - 09:20	Opening session				Exhibition
09:20 - 09:40					
09:40 - 10:00	(KEY-1) Keynote I Gerald Deboy				
10:00 - 10:20					
10:20 - 10:40					
10:40 - 11:00	Coffee break				
11:00 - 11:20	(INV-1) Invited Talk Stefano Aresu		(INV-2) Invited Talk Cezar Zota		
11:20 - 11:40					
11:40 - 12:00	Session F2-1: Power Devices Reliability: Wide-Bandgap Devices		Session B-1: Reliability for Nanoelectronics		
12:00 - 12:20					
12:20 - 12:40	Lunch Break				
12:40 - 13:00					
13:00 - 13:20					
13:20 - 13:40	Session F2-1: Power Devices Reliability: Wide-Bandgap Devices	(INV-3) Invited Talk Wenzel Prochazka	Session B-1		
13:40 - 14:00					
14:00 - 14:20		Session J: Automotive and Industrial Electronic Reliability	Session B-2: Reliability for Nanoelectronics		
14:20 - 14:40					
14:40 - 15:00					
15:00 - 15:20	Coffee break				
15:20 - 15:40					
15:40 - 16:00	Session F3: Power Devices Reliability: Power Electronic Systems	(INV-4) Best Paper IPFA26	Session B-2: Reliability for Nanoelectronics		
16:00 - 16:20					
16:20 - 16:40		Session A-1: Quality and Reliability Assessment Techniques and Methods for Devices and Systems			
16:40 - 17:00			Session C-1: Progress in Failure Analysis: Defect Detection and Analysis		
17:00 - 17:20					
17:20 - 17:40					
17:40 - 18:00	Poster Session Conference Venue				
18:00 - 18:20					
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Program Overview

2026 VIENNA ESREF

Wednesday, 23 September 2026

	Wednesday, Sept. 23rd, 2026				
	Vienna Room (EI7)	Villach Room (EI8)	Graz Room (EI9)	Linz Room (EI10)	Exhibition Area
08:00 - 08:20					
08:20 - 08:40	Registration desk opens				
08:40 - 09:00					
09:00 - 09:20	(KEY-2) Keynote II Ben Kaczer				Exhibition
09:20 - 09:40					
09:40 - 10:00					
10:00 - 10:20	Coffee break				
10:20 - 10:40	Session F2-2: Power Devices Reliability: Wide-Bandgap Devices		Session E-1: Packaging- and Assembly Reliability and Failure Analysis	(INV-5) Invited Talk Michael Rogers	
10:40 - 11:00					
11:00 - 11:20				Session G: Photonics Reliability	
11:20 - 11:40		Industrial Session			
11:40 - 12:00					
12:00 - 12:20					
12:20 - 12:40	Lunch Break				
12:40 - 13:00					
13:00 - 13:20					
13:20 - 13:40	Session F2-3: Power Devices Reliability: Wide-Bandgap Devices	Industrial Session	(INV-6) Invited Talk Francesco Iannuzzo	Session H: MEMS and Sensor Reliability	
13:40 - 14:00					
14:00 - 14:20			Session E-2: Packaging- and Assembly Reliability and Failure Analysis		
14:20 - 14:40					
14:40 - 15:00					
15:00 - 15:20					
15:20 - 15:40	Coffee break				
15:40 - 16:00					
16:00 - 16:20	Session F1: Power Devices Reliability: Smart-Power Devices and Silicon Power Devices	Industrial Session	Session E-2	(INV-7) Best Paper ISFTA25	
16:20 - 16:40					
16:40 - 17:00			Session A-2: Quality and Reliability Assessment Techniques and Methods for Devices and Systems	Session C-2: Progress in Failure Analysis: Defect Detection and Analysis	
17:00 - 17:20					
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19:00 - 19:20	Gala Dinner Main Hall Vienna				
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21:40 - 22:00					

Thursday, 24 September 2026

2026 VIENNA ESREF

	Thursday, Sept. 24th, 2026				
	Vienna Room (EI7)	Villach Room (EI8)	Graz Room (EI9)	Linz Room (EI10)	Exhibition Area
08:00 - 08:20					
08:20 - 08:40	Registration desk opens				
08:40 - 09:00					
09:00 - 09:20	(KEY-3) Keynote III Tomáš Vystavěl				Exhibition
09:20 - 09:40					
09:40 - 10:00					
10:00 - 10:20	Coffee break				
10:20 - 10:40	(INV-8) Best Paper IRPS26		Session I: Extreme Environments and Radiation		
10:40 - 11:00	Session B-3: Reliability for Nanoelectronics				
11:00 - 11:20					
11:20 - 11:40					
11:40 - 12:00					
12:00 - 12:20	Best Paper Awards and Closing session				
12:20 - 12:40					
12:40 - 13:00					Clean up Exhibition Area
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Keynote 1

Powering AI - Challenges and Solutions for Datacenters from a Reliability Perspective

Gerald Deboy
Infineon Technologies Austria AG, Austria

Time: Tuesday, 22 September 2026 at 09:30
Room: Vienna Room (EI7)

Abstract: Training of ever larger and more complex AI models requires a scaling of datacenters on three levels: first, ever larger and more powerful processors, second, clustering ever more processors in close physical proximity within the IT rack and third, forming a virtual machine with 10,000 to 100,000 processors by inter-connecting every processor to every other processor. In contrast to general purpose searches, the training of AI models is hardware-centric. Each failure of one processor forces a re-start of the training from the last stored data set. With hundreds of power devices being paralleled per processor, we need to analyze failure models under realistic pulsating load patterns and strive for an unprecedented low level of failures on device level.

The talk will explore key directions for AI datacenters and discuss the resulting reliability challenges both from a system and device-level view. Redundancy, Life time models and a system-oriented reliability methodology will be required to master these challenges ahead.



Gerald Deboy is currently a Fellow with Infineon Technologies Austria AG. He serves as a System Architect for Datacenters analyzing holistically the power flow from Grid to Core. He leads a System Innovation Group focusing on fundamental building blocks for “Powering AI”.
Dr. Gerald Deboy received the M.S. and Ph.D. degree in physics from the Technical University of Munich in 1991 and 1996 respectively. He joined Siemens Corporate Research and Development in 1992 and the Semiconductor Division of Siemens in 1995, which became Infineon Technologies later on. His research interests were focused on the development of new concepts for power devices based on the Superjunction principle. From 2004 onward he was heading the Technical marketing department for power semiconductors and ICs within the Infineon Technologies Austria AG. Since 2009 he is leading a System Innovation group specializing on new fields for power electronics with specific focus on

application cases for wide bandgap technologies. He is a Senior member of IEEE and has served as a member of the Technical Committee for Power Devices and Integrated Circuits within the Electron Device Society. In 2023 Dr. Gerald Deboy was awarded the IEEE Medal for Environmental and Safety Technologies jointly with co-recipients Dr. David Coe and Dr. Tatsuhiko Fujihira for contributions to concept and realization of Superjunction devices.
Dr. Deboy has authored and coauthored more than 100 papers in national and international journals including contributions to three student text books. He holds currently more than 100 granted international patents and has more applications pending.

Keynote 2

Technology Strategies for Evolving Compute Challenges

Ben Kaczer
imec, Belgium

Time: Wednesday, 23 September 2026 at 09:00
Room: Vienna Room (EI7)

Abstract: The rapid proliferation of large language models and agentic AI-driven applications continues to fuel an unprecedented demand for compute across datacenters and edge systems alike. The deceleration of CMOS scaling—yielding diminishing improvements in power, performance, area, and cost (PPAC) from node to node—and the escalating costs of new designs and wafer manufacturing present a dual challenge for the compute ecosystem. Addressing these constraints requires rethinking the problem from a top-down, system-level perspective, where new approaches beyond traditional scaling may be required. This talk will explore key bottlenecks limiting compute system performance: compute density, power delivery and efficiency, thermal management, and memory capacity and bandwidth. It will highlight emerging technology strategies to overcome these barriers – continued dimensional scaling, novel device architectures, new materials and innovative integration schemes using advanced interconnect technologies. The introduction of these options will need deeper understanding of failure modes with new reliability considerations. This will also require fresh approaches to failure modelling and system robustness to ensure sustained performance throughout the operational lifetime.



Ben Kaczer is a Scientific Director in the Advanced Reliability Robustness and Test (AR2T) department at imec. Dr. Kaczer received M.S. degree in Physical Electronics from Charles University, Prague, in 1992 and M.S. and Ph.D. degrees in Physics from The Ohio State University, in 1996 and 1998, respectively. In 1998 he joined the reliability group of imec, Leuven, Belgium, where his activities have included the research of the degradation phenomena and reliability assessment of SiO2, SiON, high-k, and ferroelectric films, planar and multiple-gate FETs, circuits, and characterization of Ge, SiGe, III-V, MIM, and TMD devices. He has co-authored more than 600 journal and conference papers with 20,000 citations (Google Scholar) and 5 patent groups related to device and circuit reliability, presented a number of invited papers and tutorials, and co-received 6

IEEE International Reliability Physics Symposium (IRPS) Best and Outstanding Paper Awards, 2 IEEE IPFA Best Paper Awards, and the 2011 IEEE EDS Paul Rappaport Award. Dr. Kaczer has served twice as the chair of the Characterization, Reliability and Yield subcommittee of the International Electron Device Meeting (IEDM; 2007 and 2015) and as a member of various subcommittees of the IRPS (2002—2016) IRPS management committee (2017—2026) and is currently serving as the General Chair of upcoming IRPS 2027. He was the General Chair of the Semiconductor Interfaces Specialists Conference (SISC; 2006) and continues to act as the conference secretary (2007—). He co-organized the INFOS conference (2005), and served on the INFOS, WoDiM, IPFA, and ICICDT conference committees. He has served on the Editorial Board of IEEE Journal of Transactions of Electron Devices for three terms (2011—2019).

Keynote 3

Integrated Workflows for Physical Failure Analysis

Tomáš Vystavěl
Thermo Fisher Scientific

Time: Thursday, 24 September 2026 at 09:00
Room: Vienna Room (EI7)

Abstract: As semiconductor devices become more structurally complex, physical failure analysis increasingly depends on how effectively localization, site-specific preparation, and final analytical confirmation are combined into a coherent workflow. The key challenge is not only to identify the failure site, but to move efficiently from that location to reliable root-cause determination.

This contribution outlines an integrated workflow for physical failure analysis, spanning localization, precision sample preparation, and high-resolution physical analysis. The focus is on how these steps work together to improve the success rate, reduce the time to answer, and increase confidence in the final diagnosis. Rather than concentrating on a particular device architecture, the contribution highlights a workflow-oriented approach that supports advanced semiconductor development and manufacturing.



Tomáš Vystavěl is R&D Director at Thermo Fisher Scientific, where he leads architect teams developing platforms for advanced microscopy and semiconductor workflows. His background is rooted in electron microscopy and materials characterization, with extensive experience across SEM, TEM, and FIB technologies in both research and product development. He has contributed to the development of new microscopy methods and workflow solutions across multiple application areas. He currently focuses on platform and workflow development, bringing together instrumentation, software, and application expertise to support more integrated and effective solutions.

Tutorial 1

Energy efficient power switches with Gallium Nitride technology

Srabanti Chowdhury
Stanford University, CA, USA

Time: Monday, 21 September 2026 at 13:00
Room: Vienna Room (EI7)

Abstract: GaN technology is an ever-expanding topic of research and development, proving its potential to solve several challenges in power conversion that cannot be addressed by Si. For instance, medium voltage (650-900V) devices using the HEMT configuration have been able to reduce form factor at the system level by driving circuits at higher frequencies (100kHz-1MHz) and eliminating heat sinks or reducing cooling requirements. This alone sparked the interest in GaN research to save space, energy and ultimately cost of power conversion. However, in power conversion the demand for high current from a single chip for a rated voltage is a standard need. Particularly when the market is favorable towards electrification of cars and other means of transportation, GaN must expand its scope to provide high power solutions with higher power density compared to Si, and even SiC. Vertical devices have been the choice of power device engineers for economic use of the material and maximum use of its physical properties (which allow highest possible blocking field, field mobility, etc.). GaN vertical devices, therefore, carry all the advantages offered by vertical geometry and are being explored increasingly with emphasis on material and device needs.

An overview of the achievements in vertical Gallium Nitride (GaN)-based power electronic devices will be presented with particular reference to a current aperture vertical electron transistor (CAVET), MOSFETs, Static Induction Transistor (SIT), and high voltage diodes.

Prevalent opinion suggests GaN HEMTs are suitable for 650V, while vertical devices are more suited for 1.2kV and up. In this tutorial I will build an argument to suggest how the overall (most likely system-level, but also device-level) cost would decide whether lateral or vertical devices would be the ultimate solution for power devices. Avalanche

breakdown observed due to impact ionization of carriers in vertical devices is a key reason to help make a case for the superiority of vertical devices.



Srabanti Chowdhury is a Professor in the Department of Electrical Engineering at Stanford University, with a courtesy appointment in Materials Science and Engineering. She specializes in semiconductor device engineering and leads Stanford's Wide Bandgap (WBG) Lab, where her research focuses on power conversion, delivery and advanced thermal management for computation and RF systems. She received her Ph.D. in Electrical and Computer Engineering from the University of California, Santa Barbara, in 2010. Her honors include the 2025 Quantum Device Award for pioneering contributions to vertical gallium nitride transistors and phonon-engineered interfaces; the 2023 SRC Technical Excellence Award for contributions to thermal interfaces; the 2020 Alfred P. Sloan Fellowship in Physics; and the 2016 Young Scientist Award at ISCS, along with several other early-career recognitions. She is a Fellow of the IEEE and a Senior Fellow of the Precourt Institute of Energy at Stanford University. Her lab is committed to research that directly advances energy efficiency, as well as to training the next generation of engineers and scientists to address critical challenges in energy and electronics.

Tutorial 2

CMOS product yield and reliability risk: Plasma Induced Damage (PID) past, present and future nodes

Andreas Martin
Corporate Reliability Department, Infineon Technologies AG, Germany

Time: Monday, 21 September 2026 at 13:00
Room: Graz Room (EI9)

Abstract: Plasma processing-induced charging damage (PID) is a significant yield and reliability risk for integrated circuits. A vast number of investigations have been published since the early 1990s. Prevention of PID is typically achieved through thorough process qualification and comprehensive design-rule definitions. However, in recent years, product failures related to PID have been reported in the literature for state-of-the-art technologies featuring highly isolated well configurations and complex, large-area circuits. This indicates an urgent need for refined PID design rules, which have not yet been fully adopted across the semiconductor industry.

This tutorial will present the background of PID and highlight the various failure modes associated with specific process options and circuit configurations. Examples supported by experimental data will be provided, and safe design areas for circuit designers will be defined. All topics will be discussed with reference to key publications from major international journals and conferences.

Content:

- Introduction: basic degradation mechanisms
  - Degradation and charge trapping in dielectric layers
- Failure modes
  - Metal interconnects at the gate electrode
  - Metals at source, drain, and well regions in SOI technologies
  - Well charging in isolated wells

  - MIM capacitor degradation
  - Impact of PID on metallization processes
- Detection and characterization of PID
- Circuit-level protection against PID
- Design-rule checks for products
- Standardization efforts
- Outlook: PID in advanced technology nodes



Andreas Martin received his master's degree in electronic & electrical engineering from the Technical University of Darmstadt, Germany. He worked at the Tyndall Research Institute in Cork, Ireland for several years with a focus on CMOS gate oxide reliability, before he started in 1998 in the corporate reliability department with Infineon Technologies AG in Munich, Germany. Since then, he has developed methodologies for plasma induced damage (PID) reliability qualification and fast wafer-level reliability (fWLR) monitoring for technology nodes in-house and for the foundry business. He leads PID qualification methodology and antenna design rule development at Infineon Technologies AG. He has served in the JEDEC 14.2 committee for over 25 years, where he is currently chair of the 14.2 committee and moderates three task groups: TG142_3 development of a standard on the qualification of PID gate antennas, TG142_10 standard on qualification of PID well charging, TG142_2 guideline on productive fWLR Monitoring.

Tutorial 3

Unlocking Material-to-System Innovation with AI

Hussam Amrouch
Technical University of Munich, Germany

Time: Monday, 21 September 2026 at 13:00
Room: Linz Room (EI10)

Abstract: We are entering a transformative era where AI is not only advancing our understanding of the world but also might revolutionize the design and development of semiconductor technologies and chip design. As technology scaling faces fundamental physical and reliability challenges, a holistic, material-to-system co-optimization approach is becoming essential. In this tutorial, we explore how AI can serve as a unifying force across the semiconductor design stack—from material and device optimization to system-level implementation. We demonstrate how AI algorithms can accelerate device physics simulations, enable faster development of transistor compact modeling, and offer unprecedented speed in standard cell library characterization. We highlight how AI empowers designers, for the first time, to capture and propagate awareness of aging- and defect-related phenomena—originating at the material and device level—all the way to GDSII and final sign-offs. We further discuss the critical importance of AI-driven methodologies in emerging domains such as non-volatile memories and cryogenic CMOS, where the assumptions of classical semiconductor modeling break down. Finally, we demonstrate how neural networks can be effectively employed in transistor compact models offering unprecedented speedup in SPICE simulations with an accuracy error of below 0.1%.



Hussam Amrouch is a Professor heading the Chair of AI Processor Design at the Technical University of Munich. He is the Founding Director of the Munich Advanced-Technology Center for AI Chips (MACHT-AI). He is the head of the Semiconductor Test and Reliability at the University of Stuttgart, Germany. He is the Academic Director of TU Munich Venture Lab for Semiconductor. He is the head of the Brain-inspired Computing at the Munich Institute of Robotics. He received his Ph.D. degree with the highest distinction from KIT, Germany, in 2015. He has over 330 publications, including over 135 journal articles. His multidisciplinary research covers semiconductor device physics, chip design, and computer architecture. His research interest is design for reliability, AI acceleration, emerging technologies, in-memory computing, and cryogenic circuits for quantum computing. His research in AI chips and reliability has been funded by DFG, Bavarian Ministry of Economy, Bavarian Ministry of Science, Federal Ministry of Science, Advantest, Infineon, and the U.S. Office of Naval Research.

Tutorial 4

Introduction to SiC power MOSFET Technology and Reliability

Peter Moens
onsemi Power Solutions Group, Belgium

Time: Monday, 21 September 2026 at 14:00
Room: Vienna Room (EI7)

Abstract: In this tutorial we will cover the basic aspects of both planar and trench gate SiC power MOSFET device technology and their reliability. The aim is to provide the audience with insight into the status of the reliability of SiC power devices. The following topics will be addressed:

- Characterization of the SiC/SiO2 interface by charge pumping and ultra-fast BTI measurements. From the latter the capture and emission time constant maps are derived.
- Identification of the physical nature of the interface point defects through electrically detected magnetic resonance (EDMR)
- Gate Switching instability
- Gate oxide reliability (TDDB) and lifetime. Comparison of SiC/SiO2 to Si/SiO2
- Reverse bias reliability
- Cosmic ray susceptibility
- Short circuit withstanding time
- Bipolar degradation

Finally, we will provide an outlook to “Moore’s law for power devices” and where we believe SiC will be heading into the future.



Peter Moens received a Master in nuclear physics and a Ph.D. in solid state physics from the University of Gent, Belgium, in 1990 and 1993 respectively. At onsemi is working on SiC MOSFETs. He is/was a member of the technical program committees of IEDM, ISPSD, IRPS, CSMANTECH, ICSCRM, IRW, EDTM, ESSDERC and ESREF. He was the General chair of ISPSD 2012. He authored and co-authored over 200 publications in peer-reviewed journals or conferences, 20 invited papers, and is the recipient of 6 best paper awards (including 2 ISPSD best paper awards as first author). He presented tutorials at IRPS, ISPSD, and EDTM. He is an inductee of the ISPSD International Hall of Fame. He holds 62 US patents.

Tutorial 5

Failure Analysis at a World-leading Semiconductor Manufacturer: From High Science to High-Throughput

Aidan Taylor
Infineon Technologies AG, Germany

Time: Monday, 21 September 2026 at 14:00
Room: Villach Room (EI8)

Abstract: Manufacturing semiconductor chips requires the production of thin layers (e.g. SiOx, TiN, AlN) with thicknesses down to a few monolayers over 300 mm wafers with nanometer or sub-nanometer uniformity and precision. Not only this, but composition and contamination must often be controlled into the parts-per-million range. All of this is only possible if we have the in-line control concepts, and the lab-based analysis methods that can precisely and repeatably measure these values and provide feedback. In this tutorial I will focus on the role of the failure analysis lab in this manufacturing eco-system. I will give an overview of the capabilities present in our failure analysis lab in Villach, Austria, and address the following questions:

1. What are the different roles and responsibilities of a failure analysis lab in the semiconductor industry?
2. What are the challenges faced when scaling complex measurement methods up to meet the demands of a multi-billion-euro semiconductor fab?
3. How do we address the challenge of new materials?

Aidan Taylor completed his undergraduate studies in Materials Science and Metallurgy at Cambridge University before moving to Austria where he completed a Diploma of Engineering and PhD in Materials Physics at Montanuniversität Leoben. Following his studies he worked with Dr. Budhika Mendis on quantitative electron microscopy of photovoltaic materials and with Dr. Johann Michler on the mechanical properties of thin films. Aidan was a lab manager for electron and ion microscopy at the University of California Santa Barbara, where he trained over 200

students in SEM, TEM and FIB. Since 2021 Aidan has been a failure analysis engineer at Infineon in Villach, Austria. He specializes in physical failure analysis methods and Gallium Nitride.

Tutorial 6

Reliability of Silicon-based Transistors Processed at Low Temperatures

Xavier Garros
CEA-Leti, France

Time: Monday, 21 September 2026 at 14:00
Room: Graz Room (EI9)

Abstract: 3D Sequential Integration (3DSI) is a promising alternative to continued technology scaling, enabling energy-efficient and cost-effective circuit design through the sequential stacking of active device layers. A key challenge, however, is the requirement for low-thermal-budget processing to preserve the integrity of underlying layers. This constraint raises concerns regarding the reliability of low-temperature transistors and remains a major barrier to large-scale adoption. This tutorial revisits the critical challenges associated with meeting reliability requirements for low-temperature silicon-based CMOS transistors, with a primary focus on bias temperature instability (BTI) in both n- and p-MOSFETs for digital and analog applications. A systematic investigation of the impact of thermal budget on BTI will be presented, highlighting a distinct transition in BTI behavior for processing temperatures below 600 °C. Advanced characterization and modeling techniques, including the CET map approach, will be employed to identify the oxide traps responsible for BTI in both device types. We will benchmark several process optimization strategies aimed at improving low-temperature oxide quality, including oxide growth methods, gate-stack engineering (TiN versus polysilicon), and post-deposition curing treatments such as hydrogen annealing and nanosecond laser annealing (NLA). Finally, hot-carrier reliability will be examined, with particular emphasis on the role of oxide traps in low-k spacers.



Xavier Garros is a Senior Scientist in the Silicon Technologies Department at CEA-LETI. He received his Ph.D. from the University of Marseille, France, in 2004, with a focus on the physics and electrical properties of high-k dielectrics. His expertise spans electrical characterization, device physics, and reliability modeling in advanced CMOS technologies, including bulk, FDSOI, and nanowire devices. He is currently involved in the development of 3D monolithic integration and RF technologies. He has supervised 10 Ph.D. theses and is the author or co-author of five patents and more than 160 publications in international journals and conferences in the field of CMOS physics. He has also served on the technical program committees of leading international conferences, including IEDM, IRPS, and SISC.

Tutorial 7

Degradation Physics and Degradation Rate Modeling

Joe W. McPherson
McPherson Reliability Consulting LLC, USA

Time: Monday, 21 September 2026 at 14:00
Room: Linz Room (EI10)

Abstract: Degradation physics is very important because materials degradation is a precursor to device failure. Understanding the degradation rate permits the reliability engineer to predict time-to-failure (TF) without the lengthy time required to actually measure TF. More importantly, degradation rate modeling permits the user to take corrective action before device failure actually occurs. The goal of degradation-rate modeling is to produce zero actual failures! Zero failures are incredibly important where semiconductor-related materials play essential roles in our life-support systems (fully autonomous driving vehicles, implantable medical devices, traffic controllers, space travel, etc.). All fabricated materials are metastable and will degrade with time. This is a consequence of the material changing in an effort to reach a lower Gibbs Potential. For semiconductor-related materials, degradation is normally recorded at the macroscopic level (resistance increases, leakage increases, threshold voltage increases, etc.) but the root-causes of degradation may need to be understood at the microscopic/molecular level. For any material to be successful/reliable in its intended application, the material degradation rate (as a function of use conditions: voltage, temperature, environment, etc.) must be fully comprehended. Toward this end, it is very important to understand when macroscopic models can no longer be used and a more microscopic (molecular/quantum) approach must be used for nanomaterials degradation. During this tutorial, we will investigate degradation physics and degradation rate modeling for several very important semiconductor-related failure mechanisms: time-dependent dielectric breakdown (TDDB), hot-carrier injection (HCI), bias temperature instability (BTI), electro-migration (EM), and stress migration (SM).



Joe McPherson holds a PhD degree in Physics and is an IEEE Fellow. He is widely recognized as an expert in Reliability Physics & Engineering. He has published over 200 papers on reliability physics and awarded 30 patents. He authored a reliability textbook that is widely used by students and practicing engineers: Reliability Physics and Engineering, Springer Publishing (now in its 3rd Edition, 2019). Presently, Joe is Founder & CEO of McPherson Reliability Consulting, LLC.

Session SC-1: Short Course 1 – Power Elcctronics

Chairs: Herbert Pairitsch, *Infineon Technologies Austria AG, Villach, Austria*
Michael Nelhiebel, *Infineon Technologies Austria AG, Villach, Austria*

Schedule: *Monday, 21 September 2026*
15:40 – 18:20

Room: *Vienna Room (EI7)*

(SC1-1) **Correlation of Metrology Data with Electrical Performance of Lateral p-GaN HEMT Devices**

Izabela Kuzma-Filipek
imec, Belgium

Time: Monday, 21 September 2026 at 15:40
Room: Vienna Room (EI7)

Abstract: Gallium nitride (GaN)-on-Si technology for power and RF applications requires robust defect characterization across both blanket epitaxial wafers and patterned device structures to ensure high yield, reliability, and electrical performance. A combination of optical, electron-beam, and electrical metrology techniques can provide complementary insights into defectivity at different process stages. On blanket GaN-on-Si wafers, optical inspection, photoluminescence (PL) mapping, X-ray diffraction (XRD), atomic force microscopy (AFM), and defect-selective etching are commonly employed to quantify threading dislocation density, surface morphology, stress variation, and epi-uniformity. For patterned wafers, high-resolution optical inspection, SEM review, e-beam defect inspection, scanning probe techniques, and nanoprobing enable identification of process-induced defects such as gate damage, p-GaN etch residues, metal discontinuities, particle contamination, and dielectric failures. Correlation of metrology data with electrical test results provides valuable insight into defect impact on device performance. For p-GaN

HEMTs, regions exhibiting elevated threading dislocation density or abnormal PL signatures often correlate with increased off-state leakage current and reduced breakdown voltage. Localized surface defects and gate-edge process excursions detected by patterned wafer inspection have been linked to increased gate leakage, threshold voltage variation, and reduced device yield. Additionally, defect clustering identified through optical or e-beam inspection can show strong spatial correlation with wafer-level maps of dynamic RDS(on), IDSS leakage, and early reliability failures. By combining high-sensitivity defect inspection with electrical parametric and reliability characterization, a comprehensive defect-to-performance framework can be established, enabling root-cause identification, process optimization, and improved manufacturability of p-GaN HEMT technologies.



Izabela Kuzma-Filipek received her master degree (2004) in Material Engineering from AGH University of Cracow (Poland) in collaboration with EMPA Institute (Switzerland) and her Ph.D. degree (2010) in Electrical Engineering from KU Leuven Belgium. Dr. Kuzma was a Postdoctoral Researcher at the department of Si Photovoltaics at imec and subsequently senior scientist and project manager at the same department. In 2020 Dr Kuzma started new position in GaN Power Electronic department of imec as a senior researcher and project manager. Main areas of expertise: compact devices integration, failure analysis.

(SC1-2) **Material systems for Power semiconductor switches**

Herbert Pairitsch
Infineon Technologies Austria AG, Austria

Time: Monday, 21 September 2026 at 16:10
Room: Vienna Room (EI7)

Abstract: Semiconductor switches are key components for improving the efficiency and power density of modern power electronic systems. This talk shows power switches based on different semiconductor materials, including silicon (Si), silicon carbide (SiC), and gallium nitride (GaN). In addition to material properties, the overview considers fundamentally different device concepts, particularly vertical and lateral architecture. Vertical devices offer advantages for high-voltage and high-current applications due to their scalable blocking capability and low on-state resistance. Lateral devices, in contrast, enable better System on Chip integration capability and are particularly attractive for high-frequency and integrated power applications. The different material systems provide distinct trade-offs in terms of breakdown voltage, switching speed, conduction losses, and thermal performance. Particular attention is given to the technological limits and application ranges of Si, SiC, and GaN devices including reliability aspects. The comparison demonstrates that no single semiconductor material or device concept is optimal for all power electronic applications, but the need of understanding the benefits of each for the system.

Herbert Pairitsch holds a degree in electrical engineering from the Graz University of Technology, from where he graduated in the year 1985. In 1986 he started his career at Infineon Technologies Austria AG (former Siemens HL) and held leading positions at various manufacturing and development departments. Since 2014 he served as divisional Head of R&D Funding PSS (Power and Sensor Systems). His responsibilities include the coordination of national and international research projects in the context of energy efficient electronics (e.g. LED-lighting, Smart Grids, e-Mobility) and new semiconductor materials (e.g. SiC, GaN). He held keynotes and invited talks at several conferences (e.g. IWN, PEMD, WOCSDICE, GaN Marathon).

(SC1-3) **Going beyond standard characterization: optical and e-beam methods to reveal physical properties of SiC power-devices**

Paul Stampfer
KAI/Infineon Technologies, Austria

Time: Monday, 21 September 2026 at 16:40
Room: Vienna Room (EI7)

Abstract: Silicon carbide (SiC) power MOSFETs enable efficient switching at high voltage and temperature, yet key device-physical properties are often difficult to access with standard electrical or in-line characterization alone. This short-course lecture introduces a set of complementary “non-standard” approaches that connect optical and electron-beam observables to parameters relevant for understanding and modeling modern SiC power technologies.

- Field-effect stimulated optical spectroscopy measures light emission from fully processed SiC power MOSFETs and links the emitted photons to microscopic trapping and detrapping at the / interface with direct comparison to ab-initio defect calculations.
- Quantitative secondary-electron doping contrast in the SEM converts grayscale images into two-dimensional doping maps by exploiting potential contrast and by leveraging controlled SEM conditions such as sample bias or temperature.
- Time- and frequency-resolved EBIC (Electron Beam Induced Current) methods combine periodic beam blanking and lock-in detection in a SEM to extract and map the effective carrier lifetime locally in the space-charge region of a SiC pn-junction.



Paul Stampfer leads the Device Physics group at KAI (Kompetenzzentrum für Automobil- und Industrieelektronik GmbH), a power-semiconductor research center in Villach, owned by Infineon Technologies Austria. He received his M.Sc. in Physics in collaboration with KAI and completed his Ph.D. in collaboration with ams-OSRAM, focusing on optoelectronic devices. His current research focuses on advanced electrical and optical defect-characterization techniques for semiconductor power materials and devices.

(SC1-4) **Packaging of GaN Devices for Highest Power Densities**

Ali Roshanghias
Silicon Austria Labs, Austria

Time: Monday, 21 September 2026 at 17:10
Room: Vienna Room (EI7)

Abstract: Although GaN devices offer superior switching speed, efficiency, and power density, the full exploitation of their capabilities is often hampered by conventional packaging technologies. This short course explores advanced interconnect and heterogeneous integration technologies for GaN packaging in both RF and power applications. It will address top-side interconnects in chip-on-board GaN micro-assemblies, ultra-fine-pitch flip-chip techniques, and 3D die stacking, highlighting how these approaches reduce parasitic effects, improve thermal management, and enable highly integrated, high-power-density GaN systems.



Ali Roshanghias is the head of the research unit for heterogeneous integration technologies at Silicon Austria Labs (SAL). He received his Ph.D. in materials science and technology in 2012. He pursued his career as a postdoctoral researcher in Japan and Austria in the fields of electronic materials and advanced microelectronics packaging. In 2015 he joined SAL (formerly known as CTR Carinthian Tech Research AG). He is the author of more than 100 scientific papers and patents and serves as a lecturer at the University of Klagenfurt. Ali has also served as the work package leader for integration and packaging of GaN devices in the European All2GaN project in the last 4 years.

(SC1-5) **Application needs and future application roadmap including reliability aspects**

Juraj Marek
Institute of Electronics and Photonics, Slovak University of Technology in Bratislava, Slovakia

Time: Monday, 21 September 2026 at 17:40
Room: Vienna Room (EI7)

Abstract: GaN power switches are transforming the power semiconductor industry, driven by their superior switching speed, lower conduction losses, higher power density, and improved efficiency compared with conventional silicon MOSFETs. But this transition happens slower than originally expected. This presentation shows an overview why. The application driven demand regarding the characteristics of Power semiconductor switches is shown for various types of application. This includes also effects (e.g. short circuit robustness, or dynamic on-resistance) which are influencing system concepts. It is obvious that the choice between GaN, SiC and Si is not only decided by the application, not only by the chosen topology, but by putting all aspects together including the driving scheme (and the price). Finally, this talk will take a look into a Cristal Ball taking into account these aspects.

Juraj Marek is a scientist, expert, and deputy director at Institute of Electronics and Photonics, Slovak University of Technology in Bratislava. His main areas of expertise are oriented to diagnostics and characterization methods of power devices supported by 2D/3D electro-thermal device modeling and simulation. The results of his scientific work were published in several papers in peer-reviewed journals and in numerous international conference proceedings. He participated in numerous international and national research projects (11 EU projects, 7 national projects). Currently, he is also coordinating activities in joint project with Taiwan partner ITRI focused on development of packaging pilot line at STUBA premises for SiC and ultra-WBG devices.

Session SC-2: Short Course 2 – Emerging Technologies (IEEE EDS Webinar)

Chairs: Lado Filipovic, *Institute for Microelectronics, TU Wien, Vienna, Austria*
Theresia Knobloch, *Institute for Microelectronics, TU Wien, Vienna, Austria*

Schedule: *Monday, 21 September 2026*
15:40 – 18:20

Room: *Graz Room (EI9)*

(SC2-1) **Design-Technology Co-Optimization for Reliable Integration of Emerging Memories in CMOS Circuits for Edge Computing**

Erika Covi
Technical University of Munich, Germany

Time: Monday, 21 September 2026 at 15:40
Room: Graz Room (EI9)

Abstract: Edge computing architectures require real-time data processing with minimal latency under stringent power, area, and performance constraints. The heterogeneity of edge devices and the variability in the quality of processed data call into question the validity of traditional assumptions regarding computational fungibility. This necessitates the development of specialised hardware approaches that are optimised for efficiency at the network edge. Spiking neural networks (SNNs) offer appealing advantages for edge deployment through event-driven computation, low latency, and inherent energy efficiency. However, conventional CMOS-based digital and mixed-signal implementations are faced with fundamental limitations in terms of memory density, power consumption, and area overhead, which hinder their viability for edge computing specifications. Emerging memory technologies integrated at the back-end-of-line (BEOL) of CMOS processes present a promising solution. Operating at CMOS-compatible voltages with analogue conductance modulation capability, these devices enable in-memory computing

architectures that mitigate the memory wall bottleneck by co-locating storage and computation. This approach facilitates the efficient hardware implementation of synaptic weights and neural dynamics, whilst concomitantly minimising data movement overhead. It is evident that there are still critical challenges to be addressed in order to achieve manufacturable, reliable edge computing systems. The integration of emerging devices with established CMOS flows introduces a complex process that must be managed with the utmost care. Device non-idealities, including cycle-to-cycle and device-to-device variability, endurance limitations, retention characteristics, and long-term reliability under operational stress conditions, directly impact system-level performance and require thorough electrical characterisation and modelling. Furthermore, the interdependencies between device physics, circuit design constraints, and algorithmic requirements demand rigorous design-technology co-optimization (DTCO) across the complete system stack. This presentation reports on experimental results from a tape-out integrating emerging memory devices with CMOS analogue circuits for edge computing. The present study demonstrates the critical engineering steps required for successful BEOL integration through comprehensive electrical characterisation of both individual devices and complete circuits. The present work demonstrates how concurrent development of device technology, circuit architectures, and algorithms is indispensable for the purpose of addressing integration bottlenecks, managing reliability concerns, and achieving system-level optimisation. The discussion encompasses practical trade-offs encountered during the design process, reliability considerations for ferroelectric devices in neuromorphic applications, and pathways towards manufacturable neuromorphic edge computing systems grounded in cross-layer co-optimization principles.



Erika Covi is an Assistant Professor at the Technical University of Munich (Germany), where she leads the Nanoelectronics Circuits and Systems (NCAS) Group. She received her Ph.D. in Microelectronics from the University of Pavia (Italy) in 2014. Following her doctoral studies, she was a researcher at the National Research Council (CNR) of Italy and Politecnico di Milano (Italy). She was later Senior Scientist at NaMLab gGmbH in Dresden, Germany, and Assistant Professor at the University of Groningen (the Netherlands). Her research focuses on the intersection of emerging memory devices, circuit design, and brain-inspired computing, with an emphasis on design-technology co-optimization (DTCO). Her work explores how the intrinsic physical properties of novel memory technologies can be leveraged to develop energy-efficient computational systems by integrating emerging memory devices with CMOS circuits. She has been awarded with the ERC Starting Grant in 2021 and the ERC Proof of Concept in 2025.

(SC2-2) **Two-Dimensional FETs for Logic and Beyond: Scaling, Integration, and New Computing Paradigms**

Saptarshi Das
Pennsylvania State University, USA

Time: Monday, 21 September 2026 at 16:10
Room: Graz Room (EI9)

Abstract: Two-dimensional (2D) semiconductors have emerged as a compelling platform for extending field-effect transistor (FET) scaling while simultaneously enabling new computing paradigms beyond conventional CMOS. In this tutorial, I present a device-to-system perspective on 2D FET technologies, drawing on three recent demonstrations from my group that span logic, scaling, and in-memory computing. I first discuss complementary 2D transistor integration through a monolithic one-instruction-set computer, highlighting how wafer-scale 2D CMOS can support non-traditional architectures with minimal hardware overhead. I then examine aggressively scaled MoS_2 FETs with sub-35 nm channel and contact lengths, focusing on electrostatics, contact engineering, and the implications for ultimate logic scaling. Finally, I present large-scale crossbar arrays based on three-terminal MoS_2 memtransistors, illustrating how 2D FETs can simultaneously serve as memory and computing elements for neuromorphic and probabilistic hardware. Together, these examples underscore how 2D FETs are not only viable replacements for scaled silicon devices, but also key enablers of tightly integrated logic–memory architectures and emerging computing models.

Short Course 2 – Emerging Technologies



Dr. Das received his B.Eng. degree (2007) in Electronics and Telecommunication Engineering from Jadavpur University, India, and his Ph.D. degree (2013) in Electrical and Computer Engineering from Purdue University. He was a Postdoctoral Research Scholar (2013-2015) and Assistant Research Scientist (2015-2016) at Argonne National Laboratory (ANL). Dr. Das joined the Department of Engineering Science and Mechanics (ESM) at Penn State University in January 2016. Dr. Das received the Young Investigator Award from the United States Air Force Office of Scientific Research in 2017 and the National Science Foundation (NSF) CAREER award in 2021. Das Research Group at Penn State focuses on 2D microelectronics for monolithic 3D integration, bio-inspired sensing, neuromorphic computing, and hardware security.

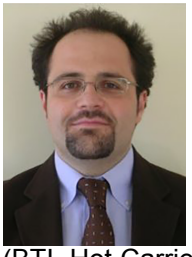
(SC2-3) **Gate Stack Stability Challenges of Emerging MOS Device Technologies**

Jacopo Franco
imec, Belgium

Time: Monday, 21 September 2026 at 16:40
Room: Graz Room (EI9)

Abstract: The unabated performance enhancement of semiconductor technology has been sustained in recent years by disruptive device and material innovations. For the successful deployment of any novel device concept, the promised enhanced performance must be guaranteed for the entire expected lifetime of the final product. Traditionally, device reliability optimization was an aspect considered only at a late stage in the development of a new device technology. We argue that in contemporary devices, fabricated with complex integrations and a plethora of materials, potential reliability issues should be considered from the very early stage of the technology development, as they can potentially disqualify otherwise promising device concepts. In particular, charge trapping in gate dielectrics is an aspect that can “make or break” any MOS-based device, and thus gate stack stability should be considered as a primary metric in the evaluation of novel device concepts. In this talk, we will review the fundamentals of charge trapping in gate dielectrics in terms of phenomenology, characterization techniques, and physical models. Next, we will briefly discuss, as case studies, some recent examples of MOS innovations which made it into mainstream technology (e.g., SiGe channels), as well as other examples which to date remain confined to academic research (e.g., III-V and Ge channels for Logic). We will then focus on specific gate stack challenges for upcoming CMOS technology innovations, including Nanosheet and Forksheet device architectures, and novel device concepts such as the stacked Complementary FET (CFET) and 2D channel transistors. Finally, we will discuss novel transistors based on oxide semiconductor channels (e.g., IGZO), which due to their extremely low off-state leakage and their flexible fabrication flow, are considered as potential gamechangers for memory periphery and, in general, for the heterogeneous integration of transistors in the Back End of Line (BEOL). For these devices, we will discuss how the interplay between their gate dielectric and channel instabilities makes the reliability assessment and optimization particularly complex, requiring a combination of electrical and optical characterization techniques.

Short Course 2 – Emerging Technologies



Jacopo Franco is a Principal Member of Technical Staff in the Reliability group of imec, Belgium. He received the B.Sc. (2005) and M.Sc. (2008) from U. Calabria - Italy, and the Ph.D. degree from KU Leuven - Belgium (2013) in Electrical Engineering. His research focuses on CMOS FEOL reliability characterization, optimization, and modelling, and in particular: i) on gate stack development for novel device technologies (SiGe, Ge, III-V, IGZO), novel architectures (finFETs, FD-SOI, Nanowires, Nanosheets), and novel integration schemes (Sequential 3D tier stacking, CFETs); ii) on characterization and physics-based modelling of FEOL degradation mechanisms (BTI, Hot Carrier, Off-state degradation, TDDB, RTN, Time-Dependent Variability). He has (co)authored 300+ papers and 4 patent families, and he is a (co-)recipient of 8 IEEE awards. He has been serving in various functions on the Committees of IRPS, SISC, IIRW, ESREF, WoDiM and INFOS conferences, and as an Associate Editor of IEEE T-DMR and T-ED.

(SC2-4) **Resistive-switching RAM reliability from device to system**

Cristian Zambelli
Università degli Studi di Ferrara, Italy

Time: Monday, 21 September 2026 at 17:10
Room: Graz Room (EI9)

Abstract: As the demand for high-performance, low-power non-volatile memory (NVM) grows, Resistive-switching Random Access Memory (RRAM) has emerged as a leading candidate for the next generation of Storage Class Memories (SCM). By bridging the performance gap between DRAM and Flash, RRAM offers the potential for high-speed operation, high-density integration via $4F^2$ cross-point arrays, and low-power consumption. However, the path to widespread commercial adoption is complex, requiring a holistic understanding of reliability that spans from fundamental device physics to complex system-level management. This talk provides a comprehensive overview of RRAM reliability, focusing on Redox-based RRAM (OxRAM) using Hafnium oxide (HfO2) technology. At the device level, RRAM operation relies on the formation and disruption of a conductive filament (CF) composed of oxygen vacancies. While this mechanism enables high scalability, it is inherently stochastic. The choice of materials—such as amorphous versus poly-crystalline oxides—and the deposition chemistry (e.g., halide-based vs. metal-organic precursors) significantly influence the initial “Forming” process and the subsequent “Set” and “Reset” windows. We explore how the compliance current acts as a critical lever for controlling filament size, which in turn dictates the trade-off between power consumption and state stability. The core of RRAM reliability challenges lies in the dynamic nature of the conductive filament. We analyze the primary failure mechanisms: endurance, retention, and variability. Endurance is limited by the physical degradation of the oxide due to repetitive oxygen ion migration, where “Over-SET” or “Over-RESET” conditions can lead to permanent device wear. Retention, particularly at high temperatures, is threatened by the out-diffusion of vacancies, which causes the Low Resistance State (LRS) to drift toward a High Resistance State (HRS). Furthermore, we address the significant hurdle of variability, both device-to-device and cycle-to-cycle. This variability is compounded by phenomena such as Resistance Drift and Random Telegraph Noise (RTN), which pose severe risks to the stability of Multi-Level Cell (MLC) operations. To transition from a single cell to a functional system, these reliability “quirks” must be mitigated through architectural innovations. We

discuss system-level strategies, including iterative program-and-verify algorithms to tighten resistance distributions and periodic content re-mapping to handle retention loss. The talk concludes by examining how these reliability considerations shape RRAM's role in emerging applications. From automotive microcontrollers requiring extreme thermal stability to in-memory computing (IMC) architectures where RRAM serves as an analog synaptic weight, understanding the reliability chain from the atomic level to the system level is paramount for the future of emerging memory technologies.



Cristian Zambelli received the M.Sc. and the Ph.D. degrees in Electronic Engineering from the University of Ferrara, Ferrara, Italy, in 2008 and 2012, respectively. Since 2022, he holds an Associate Professor position with the same institution. His current research interests include the electrical characterization, physics, and reliability modeling of different nonvolatile memory technologies at the array level. He is also interested in the evaluation of the Solid-State Drives reliability/performance trade-offs exposed by the integrated memory technology and in neuromorphic computing using heterogeneous accelerators such as FPGAs and In-Memory Computing architectures.

(SC2-5) **Defect engineering in emerging memristive devices for neuromorphic computing**

Lambert Alff
Technische Universität Darmstadt, Germany

Time: Monday, 21 September 2026 at 17:40
Room: Graz Room (EI9)

Abstract: The memristor has been predicted as a fourth passive circuit element in the seventies of the last century and subsequently discovered only after the year 2000. The resistance of a memristor “remembers” the current that has passed through it by a change in the resistive state. At sufficiently low voltages, the resistance can be read without changing the state. The first generation of memristive devices focused on non-volatile digital memory using a high and low resistive state. More recently, analog computing has become relevant in particular for neuromorphic computing where matrix vector multiplications are essential. Here, the resistive state of the memristor represents the weights of the matrix elements and can be ideally changed in a linear way (depression and potentiation). More than that, memristors can fulfill synaptic functions making them highly interesting for brain-inspired computing. The key challenge in the application of memristors is their stochastic switching behavior from cycle-to-cycle and device-to-device. This talk focusses on oxide memristors where the manipulation of a conducting filament governs the resistance state. We discuss the materials science of defects in HfO2 and Y2O3-based memristors and their characterization by advanced methods including operando transmission electron microscopy.

Short Course 2 – Emerging Technologies



Lambert Alff has studied physics at the University of Tübingen on the topic of high-tempertature superconductors and their devices. After a Feodor Lynen fellowship in Tsukuba, Japan, he returned for his habilitation to the University of Cologne where he started to work on tunnelling magnetoresistance devices. He changed to TU München where he became a founding member of a CRC on solid state quantum computation. He served as a full professor on Materials for electrical engineering at the Technical University of Vienna in the electrical engineering department. He currently is a full professor for Advanced Thin Film Technology at Technische Universität Darmstadt with a focus on materials for memristive and high-frequency devices. He has published more than 250 peer reviewed papers and supervised more than 30 PhD theses.

Invited Talks

(INV-1) **Enabling Large Scale Implementation of Reliable WBG Devices from a Manufacturer's Viewpoint**

Stefano Aresu
Infineon Technologies, Austria

Time: Tuesday, 22 September 2026 at 11:00
Room: Vienna Room (EI7)

Abstract: Wide bandgap (WBG) power semiconductors give significant advantages, but they also introduce new reliability risks and qualification demands. This talk highlights the challenges specifically shared by SiC Vertical MOSFETs and GaN Lateral HEMTs. Understanding the reliability limits of both technologies is important to meet the low-DPPM levels expected by customers and already achieved by mature Silicon MOSFETs. Dedicated dynamic measurements are needed to reveal new degradation mechanisms and develop related failure models. In addition, there is the desire to provide universal degradation models for each technology to be applied to a large portfolio of products with a variety of designs and application-relevant needs. These insights shape our qualification strategy as a company and the demand for tailored industry-wide WBG standards. Managing extreme thermal and electrical stress during dynamic testing is particularly challenging, but it is important to balance manufacturing constraints with strict reliability targets. The SiC Vertical MOSFET shows its advantages in high-voltage and high-power applications, leveraging high thermal conductivity and moderate-to-high switching frequencies. We review its primary degradation mechanisms and discuss reliability tests used to evaluate its robustness under realistic operating conditions. Particular attention is given to gate oxide degradation, interface state generation, threshold voltage instability, and degradation induced by repetitive switching stress. While high temperature blocking condition and gate stress are primarily used to assess static reliability and gate oxide robustness, gate switching stress and other dynamic tests are essential for investigating mechanisms that arise under application-relevant switching conditions, as well as for defining production screening limits and guard bands to ensure the highest quality. Similar to the SiC MOSFET, the GaN Lateral HEMT also requires dynamic testing to capture degradation occurring only under switching stress. GaN devices show their advantages for medium-voltage and medium-power applications with their ultra-low specific on-resistance and ultra-high switching frequencies. Operating under extreme conditions

introduces degradation mechanisms that a traditional qualification strategy may not reveal. Characterizing these mechanisms can ensure high reliability for large-scale deployment.



Stefano Aresu received his degree in electronic engineering from the University of Cagliari in 2000. He then joined IMEC, where he focused on hot carrier effects in power devices. After earning his Ph.D. in physics in 2005, he joined the Central Reliability Department at Infineon Technologies as a Reliability Engineer responsible for qualifying automotive and industrial power devices. His research included investigations on NBTI and hot carrier effects as well as the development of device life time models. Over the past few years, he has been responsible for process qualifications and transfers for advanced smart power technologies. As a Lead Principal Engineer, he currently serves as the overall coordinator for front-end reliability topics, implementing methods ranging from single devices to full products, including eFlash and RRAM memories. He is the author and co-author of over 30 papers and patents in microelectronics reliability and actively contributes to JEDEC and AEC-Q100 standards.

(INV-2) **Cryogenic Low-Noise Amplifiers for Quantum Computing: Engineering Noise and Thermal Properties**

Cezar Zota
IBM Research Europe, Switzerland

Time: Tuesday, 22 September 2026 at 11:00
Room: Graz Room (EI9)

Abstract: Cryogenic low-noise amplifiers are essential parts of today's quantum computers and are primarily employed in the readout path at the 4 K stage to read the qubit states. Their performance and reliability directly impact the quantum computations, e.g. through the readout fidelity. As one of the few active, i.e. power-dissipating, cryogenic devices used already today, there are strict requirements placed in terms of noise-levels, power, stability and robustness. To support ever increasing qubit numbers, improved amplifiers will be desirable in the future. In this presentation, we demonstrate our cryogenic III-V high-electron mobility transistor technology based on the InGaAs/InP system. We show how noise properties depend on temperature, and how this dependence arises from various traps and defects across the heterostructure that can be effectively suppressed with quantum well engineering. We also describe thermal effects, in particular self-heating, which is one of the primary limits of noise and reliability in these devices. Several self-heating measurement methodologies are examined, such as quantum thermometry, which is able to determine both the intrinsic electron temperature and associated scattering mechanisms throughout the device self-heating process.



Cezar Zota received the PhD degree in Electrical Engineering from Lund University, Sweden, in 2017. Since then, he has been a Staff Research Scientist and Master Inventor at IBM Research Europe – Zurich. His research interests include cryogenic electronics for quantum computing, including III-V amplifiers, cryo-CMOS, and cryogenic modelling. More recently, his work has also focused on state-of-the-art CMOS technologies, in particular for the back-end-of-line. He is the recipient of an Ambizione career grant from the Swiss National Science Foundation, is a member of the National Centre of Competence in Research SPIN, has coordinated several European research projects, and holds over 20 patents and has co-authored over 80 peer-reviewed publications in the field of electron devices.

(INV-3) **Automotive Battery Management Chipset, In-field, Maintenance & Lifetime**

Wenzel Prochazka
NXP Semiconductors Austria GmbH, Austria

Time: Tuesday, 22 September 2026 at 13:20
Room: Villach Room (EI8)

Abstract: High precision voltage measurements qualified for >15 years, backed with a safety certified system layout, cybersecurity and combined with cost effective wireless capability, are needed for modern EV powertrains to meet customer expectations. NXP's Battery Management Chipset reference design supports maximizing battery longevity by combining multiple technologies not only as begin-of-life datasheet specifications. This presentation gives some insights into how we can achieve this.



Wenzel Prochazka has nearly 20 years background in EV Battery and powertrain development activities, before he joined NXP in 2023 to manage the electrification system products elaboration. Today Dr. Wenzel Prochazka manages the process of NXP systems for HV batteries and enabling customers of NXP with a large part of the value share in innovative system solutions in processing and analog controls for HV EV powertrains.

(INV-4) **Picosecond Pulse Generation Methods for Die-to-Die ESD Testing (Best Paper Award at IPFA 2026)**

Christian Herpers
Fraunhofer EMFT

Time: Tuesday, 22 September 2026 at 15:40
Room: Villach Room (EI8)

Abstract: Due to miniaturization and heterogeneous integration of chiplets in the semiconductor industry, a need for electrostatic discharge (ESD) testing of die-to-die (D2D) interfaces has emerged. Current ESD testing methods, such as transmission line pulsing with switching relays, cannot reliably replicate fast D2D ESD events. Hence, novel pulse generation schemes reducing the transition time to below 50 ps are required. This work presents two methods of picosecond pulse generation with broadband radio-frequency amplification for D2D ESD testing. A high-speed arbitrary waveform generator is leveraged to generate short pulses achieving transition times down to 6.4ps and amplitudes up to 28V after amplification. Pulse generation with step recovery diodes yields transition times below 30 ps and amplitudes up to 19 V after amplification. While pulse generation with step recovery diodes is simple, less costly, and yet effective, the approach using high-speed arbitrary waveform generation shows overall better results. The presented pulse generation methods can be applied to future ESD testing of D2D interfaces in heterogeneously integrated devices.



Christian Herpers received his B.Eng. in electrical engineering and information technology from the Munich University of Applied Sciences, Munich, Germany, in 2022 and completed his M.Sc.E. in electrical engineering at the University of New Brunswick, Fredericton, NB, Canada, in 2023. From 2017 to 2022, he was a Dual and Working Student with Rohde & Schwarz, Munich and from 2022 to 2023, a Research and Teaching Assistant with the University of New Brunswick. Since 2024, he has been with the Technical University of Munich and joined the Fraunhofer EMFT Institute for Electronic Microsystems and Solid State Technologies as a Research Assistant in 2025. His research interests include electrostatic discharge, RF measurements, and wireless power.

(INV-5) **From Device Reliability to System Reliability: Challenges Across the Photonics Value Chain**

Michael Rogers
ams OSRAM AG, Austria

Time: Wednesday, 23 September 2026 at 10:20
Room: Linz Room (EI10)

Abstract: Digital photonic products are increasingly complex systems comprising semiconductor devices, optical post-processing layers, advanced packaging technologies, interconnect structures, and optoelectronic assemblies. While significant progress has been made in understanding the reliability of individual photonic components—including LEDs, VCSELs, photodiodes, and SPADs—industrial experience shows that many field reliability issues originate from downstream processing, component integration, and system-level interactions. This presentation examines reliability from a broader product perspective, addressing the complete photonics value chain, from device fabrication to long-term performance in end applications. Particular emphasis is placed on reliability risks introduced during downstream processing and system integration. Examples include silicon post-processing technologies such as through-silicon vias (TSVs), color and interference filters, handling- and assembly-induced defects, interconnect degradation, corrosion phenomena, contamination effects, and package-induced thermomechanical stresses. These mechanisms can create latent defects or accelerate degradation processes that become apparent only during prolonged environmental exposure or field operation. Through selected industrial examples, the presentation illustrates how reliability risks evolve and propagate across increasingly integrated photonic products. Particular attention is given to the interfaces between semiconductor devices, optical post-processing layers, interconnect technologies, packaging elements, and other structural components of the system architecture. The discussion demonstrates how interactions among these elements can create complex failure paths that may not be evident when components are assessed in isolation. In some cases, system-level reliability requirements and integration-related failure mechanisms ultimately necessitate changes to the design of individual components, highlighting the strong interdependence between device design and product architecture. Building on these observations, the

presentation highlights the importance of understanding the physical architecture of photonic systems. Reliability risks frequently originate at interfaces where optical, electrical, thermal, mechanical, and environmental sensitivities interact, creating cross-dependencies that may remain hidden when components are evaluated independently. A thorough understanding of component sensitivities, interface behavior, and resulting cross-dependencies is therefore essential for identifying and mitigating system-level failure mechanisms. Risk-management methodologies such as DFMEA are valuable tools, but their effectiveness ultimately depends on a sound understanding of the underlying architecture and interaction mechanisms. This broader perspective supports a shift from a purely component-centric view of reliability toward a system-level understanding of photonic products. By linking physical degradation mechanisms to architectural interfaces and component interactions, reliability can be assessed in terms of customer-relevant outcomes such as sensitivity loss, accuracy degradation, parametric drift, reduced signal-to-noise ratio, or catastrophic failure. This perspective provides a more effective framework for identifying and mitigating reliability risks in increasingly integrated photonic systems. While component reliability remains the foundation of robust photonic products, increasingly integrated systems demand a broader reliability perspective. Understanding system architecture, component interfaces, and integration-related interactions is essential for managing reliability risks and preserving functional performance throughout product lifetime. Meeting future challenges will require a holistic reliability approach spanning the entire photonics value chain—from device physics to system architecture.



Michael Rogers is Senior Director of Quality and Head of Technology Quality Engineering at ams OSRAM, where he is responsible for quality engineering in new technology development and leads the global reliability and failure analysis laboratories for the Light Sensing and Photonics business. He received a Diplomingenieur degree (equivalent to an MSc) in Technical Chemistry, a Doctorate in Technical Physics, and a Master of Advanced Studies in Nanotechnology and Nanoanalytics from Graz University of Technology. He began his career in electron microscopy and semiconductor failure analysis, specializing in focused ion beam (FIB), transmission electron microscopy (TEM), and advanced materials characterization. Since joining ams OSRAM in 2007, he has held roles spanning defect engineering, process integration, product reliability, and global quality and reliability leadership. His professional interests include semiconductor reliability, optical sensing technologies, failure analysis, and reliability engineering across the photonics value chain.

(INV-6) **Ultra-Reliable All-Liquid Interconnections for Power Electronics Components**

Francesco Iannuzzo
Polytechnic of Turin, Italy

Time: Wednesday, 23 September 2026 at 13:20
Room: Graz Room (EI9)

Abstract: Power semiconductors are vulnerable to thermo-mechanical stress due to the use of solid-metal interconnect technologies such as wire bonding, soldering, and sintering. This presentation showcases a successful usage of room-temperature Gallium-based liquid-metal pastes for chip-level packaging of SiC MOSFETs. All chip-critical interconnects (die-attach, topside, and gate connections) are implemented using liquid-metal, which remains liquid during operation. We tested the SiC MOSFETs for thermal and reliability performance. Liquid-metal packaged SiC MOSFETs showed improved thermal performance and an order of magnitude increase in power cycling lifetime. Notably, the liquid-metal pastes are contained without the use of any encapsulation.



Francesco Iannuzzo is a professor of reliable power electronics with the Power Electronics Innovation Center (PEIC) at Politecnico di Torino, Italy. His research focuses on the reliability of wide-bandgap power devices (SiC MOSFETs, GaN HEMTs), their modeling and characterization, condition monitoring, simulation, and new driving concepts to improve reliability. Prof. Iannuzzo is the author or co-author of over 350 publications in journals and international conferences, five book chapters, and an edited book on Modern Power Electronic Devices. He has delivered over 50 technical seminars, keynotes, and several invited speeches on power electronic device reliability at top-tier conferences, including ISPSD, IRPS, EPE, ECCE, PCIM, and APEC. Furthermore, he is a Fellow of the U.S. Institute of Electrical and Electronics Engineers (IEEE). He has served as General Chair of ESREF 2018, IWIPP 2022 (International Workshop on Integrated Power Packaging), and EPE-ECCE Europe 2023.

Invited Talks

(INV-7) **Active Auto Thinning (AAT): An AI-Driven Autonomous FIB Endpointing Method Based on Cut-Face Probability Inference and Image Interpolation for Advanced Memory Devices (Best Outstanding Paper Award at ISTFA 2025)**

Bryan Sang Hoon Lee
Micron Technology, USA

Time: Wednesday, 23 September 2026 at 16:00
Room: Linz Room (EI10)

Abstract: As semiconductor memory technologies continue to scale into the sub-10 nm regime, accurate endpoint determination during focused ion beam (FIB) thinning has become a critical challenge for transmission electron microscopy (TEM) sample preparation and failure analysis. Conventional passive auto thinning (PAT) workflows rely on predefined fiducials and operator interpretation of processed scanning electron microscopy (SEM) images, limiting endpoint precision and increasing susceptibility to process variability, beam instability, and human error. This study presents an autonomous FIB thinning methodology, termed Active Auto Thinning (AAT), that integrates machine vision, artificial intelligence (AI), probability-based endpoint prediction, and image interpolation algorithms for real-time control of FIB milling in advanced DRAM and NAND devices. The proposed framework utilizes sequential Slice-and-View SEM datasets to reconstruct three-dimensional device geometry and train AI models capable of recognizing evolving cross-sectional features as milling progresses. Rather than relying on image data optimized for human visualization, the system analyzes detector-derived information directly, preserving high-frequency structural information and enabling enhanced endpoint sensitivity. During operation, probability maps generated from real-time SEM images are combined with interpolation-based distance estimation to predict the remaining distance between the current cut face and the target region of interest. A closed-loop control architecture continuously updates process parameters and autonomously determines milling termination conditions. Experimental validation was performed using advanced FIB-SEM platforms and applied to leading-edge memory devices. The AAT workflow demonstrated reliable identification of target cut faces, robust compensation for beam and process variations, and autonomous

operation without operator intervention. Compared with conventional PAT methods, AAT produced thinner and more uniform TEM lamellae, achieving specimen thicknesses near 10-20 nm while maintaining nanometer-scale endpoint accuracy. Statistical evaluation across multiple DRAM samples yielded an average lamella thickness of 15.3 nm with a 2σ variation of 1.26 nm and target-centering accuracy within 0.72 nm (2σ). The resulting TEM specimens exhibited reduced three-dimensional projection effects, improved critical-dimension metrology capability, and enhanced structural fidelity. The implementation of AAT represents a transition from automated to truly autonomous FIB sample preparation by enabling dynamic decision-making based on real-time image inference rather than fixed process scripts. The methodology improves throughput, repeatability, and data quality while reducing dependence on operator expertise. These results demonstrate the feasibility of AI-driven autonomous endpoint detection and establish a foundation for scalable, high-throughput semiconductor failure analysis and future unmanned laboratory environments.



Bryan Sang Hoon Lee is a Principal Engineer in the Yield Enhancement and Technology Laboratory at Micron Technology (USA), where he develops advanced failure analysis and characterization solutions for next-generation memory devices. His expertise includes focused ion beam (FIB) technologies, transmission electron microscopy (TEM), machine vision, and AI-driven process automation for advanced memory device applications. Prior to joining Micron in 2021, he spent a decade at FEI Company (now Thermo Fisher Scientific), contributing to advanced FIB/SEM technologies and materials characterization solutions. Dr. Lee holds M.S. and Ph.D. degrees in Materials Science and Engineering from Seoul National University and The University of Texas at Dallas. His recent work focuses on autonomous laboratory workflows and real-time process control. Dr. Lee has authored and presented numerous technical papers at international conferences, including ISTFA, commercialized multiple patented technologies, and continues to advance autonomous failure analysis technologies for semiconductor manufacturing.

(INV-8) **Reaching the BTI 10yrs Lifetime for 2.5V BEOL Compatible (<420°C) High Voltage Si-CMOS (Best Paper Award at IRPS 2026)**

William Vandendaele
CEA-Leti

Time: Thursday, 24 September 2026 at 10:20
Room: Vienna Room (EI7)

Abstract: This paper investigates process options to fabricate reliable 420°C full Si CMOS high voltage transistors (reaching BTI 10yrs limit for both P/NMOS). The analysis of TiN based and Si-POLY gate with UV nanosecond laser annealing (UV-NLA), proves that TiN on SiO_2 even at 420°C is not reliable due the O-scavenging (detrimental for NBTI). Si-POLY gate using UV-NLA activation with 420°C high pressure passivation (HPD2) reaches the 10yrs limit at VOV = 2.3V (VG = 2.5V) for both P/NMOS without hydrogen radical annealing (H*), benefiting of UV-NLA fast high temperature transients. The interface traps creation during NBTI relies on gate materials concerning PMOS and, on passivation scheme for NMOS during PBTI stress. The analysis of CET maps suggests a significant reduction of H-E' in SiO2, both for electron (-/0) and holes (0/+) traps using high pressure passivation.



William Vandendaele received the M.Sc. ('07) degree in nanomaterial sciences at Grenoble INP and the Ph.D. degree from University of Grenoble-Alpes ('10) in microelectronics. He joined SOITEC in 2011 where he was head of the electrical characterization of the R&D department. Between 2014 and 2023, he is in charge of the electrical characterization, tests and reliability of GaN based substrates and devices for power electronics at CEA-LETI. Since 2023, he is involved in the development of 10nm FDSOI, Low Temperature SOI and Si-Photonics technologies as a characterization and reliability expert leading a small group of engineers and students. He has authored of more than 60 papers in international conferences or journals and holds 5 patents. He has been awarded with the IEEE IRPS 2018 and 2026 best papers. He is a former member of the RSD IEEE IEDM subcommittee and current member of the IEEE IRPS Gate/MOL subcommittee and ESREF. He has been a TPC member of IWN, GaN Marathon. He serves as regular reviewer for IEEE TED, EDL and Microelectronic Reliability.

Session IND: Industrial Session

Schedule: *Wednesday, 23 September 2026*
11:20 – 17:20
Room: *Villach Room (EI8)*

11:20	(IND-A5) **Eurofins MASER B.V.** Booth A5	eurofins | MASER
11:40	(IND-B11) **TrInity Analysis Tech Co., Ltd.** Booth B11	衡儒分析科技股份有限公司 Trinity Analysis Tech., Co., Ltd TIA TRINITY ANALYSIS
12:00	(IND-C3) **scia Systems GmbH** Booth C3	scia systems
13:20	(IND-A2) **JP Kummer Semiconductor Technology** Booth A2	KUMMER SEMICONDUCTOR TECHNOLOGY

Industrial Session

13:40	(IND-A3) **Kleindiek Nanotechnik** Booth A3	
14:00	(IND-A6) **Imina Technologies SA** Booth A6	
14:20	(IND-B2) **Microsanj** Booth B2	
14:40	(IND-B3) **Seiwa Optical Europe** Booth B3	
15:00	(IND-B5) **QZabre** Booth B5	
16:00	(IND-B6) **F&S BONDTEC Semiconductor** Booth B6	

16:20	(IND-B7) **SECTOR TECHNOLOGIES SAS** Booth B7	SECTOR TECHNOLOGIES	
16:40	(IND-B12) **QuantumDiamonds** Booth B12	QUANTUM DIAMONDS SENSOR TECHNOLOGY	
17:00	(IND-C1) **JEOL (Germany)** Booth C1	JEOL	

Session A-1

Session A-1: Quality and Reliability Assessment Techniques and Methods for Devices and Systems (Devices)

Chairs: Cora Salm, *University of Twente, Netherlands*
Edgar Olthof, *NXP Semiconductors, Netherlands*

Schedule: *Tuesday, 22 September 2026*
15:40 – 18:00

Room: *Villach Room (EI8)*

15:40 (INV-4) **Picosecond Pulse Generation Methods for Die-to-Die ESD Testing (Best Paper Award at IPFA 2026)**
Christian Herpers
Fraunhofer EMFT, Germany

16:00 (A-1-1) **Coupling On-Chip Sensor with a Control and Repair Strategy to Monitor Memory Aging Evolution**
Fabian Vargas[1], Vache Galstyan[2], Gurgen Harutyunyan[2], Yervant Zorian[3]
[1] *IHP - Leibniz Institute for High Performance Microelectronics, Germany;* [2] *Synopsys, Armenia;* [3] *Synopsys, United States*

16:20 (A-1-2) **Robustness of Memristor-Based Neuromorphic Inference under Stuck-at Faults and Variability**
Hassen Aziza[1], Hanzhi Xun[2], Moritz Fieback[2], Mottaqiallah Taouil[2], Said Hamdioui[2], K. Coulié[1], W. Rahajandraibe[1]
[1] *Aix-Marseille University, France;* [2] *Delft University of Technology, Netherlands*

16:40 (A-1-3) **Characterisation of Leakage Current in Multilayer Bulk PZT Actuators**
Ruth Houlihan, Anina Anju Balaraman, Russell Duane
Tyndall National Institute, Ireland

17:00 (A-1-4) **Stochastic Aging Trajectory Prediction for LEDs under Different Aging Conditions**
Andreas Zippelius, Elias Hufnagel, Gordon Elger
Technische Hochschule Ingolstadt, Germany

17:20 (A-1-5) **Correlation of structural and electronic properties in (Al)GaN Heterostructures by Multi-mode Scanning X-ray Microscopy**
Agnieszka Corley-Wiciak[1], Fleur Voortman[2], Manuel Stabentheiner[3], Laura Neumann[4], Pierre Everaere[1], Ennio Capria[1], Thu Nhi Tran Caliste[1], Michael Reisinger[5], Tobias Schulli[1], Cedric Corley-Wiciak[1]
[1]*ESRF - European Synchrotron Radiation Facility, France;* [2]*University of Twente, Netherlands;* [3]*Infineon Technologies Austria AG, Austria;* [4]*Fraunhofer IKTS, Germany;* [5]*KAI GmbH, Austria*

17:40 (A-1-6) **Not All Upsets Are Equal: A Measured Test of whether SECDED suffices for Radiation-Exposed COTS Memory**
Md Saad Memon[1], Rafal Graczyk[2], Jan Swakon[3], Leszek Grzanka[3], Sebastian Kusyk[3], Mike Papadakis[1]
[1]*University of Luxembourg, Luxembourg;* [2]*Independent Researcher, Luxembourg;* [3]*Institute of Nuclear Physics Polish Academy of Sciences (IFJ PAN), Poland*

Session A-2

Session A-2: Quality and Reliability Assessment Techniques and Methods for Devices and Systems (Systems)

Chairs: Cora Salm, *University of Twente, Netherlands*
Edgar Olthof, *NXP Semiconductors, Netherlands*

Schedule: *Wednesday, 23 September 2026*
16:40 – 18:00

Room: *Graz Room (EI9)*

16:40 (A-2-1) **Time Series-based On-Chip Prediction of Aging and Power Supply Noise-induced Delay Degradation**
Nikolaos Zazatis[1], Konstantinos Varakliotis[1], Aikaterini Tsilingiri[1], Konstantinos Andrikopoulos[1], Christos Sotiriou[1], Marko Andjelkovic[2], Fabian Vargas[2]
[1] *University of Thessaly, Greece;* [2] *IHP, Germany*

17:00 (A-2-2) **Generic Failure Rates Based on VITA 51.1 S2025 and AI-Assisted Reliability Prediction**
Gernot Riedel, Yogesh G-V, Jürgen Schuderer
Hitachi Energy, Switzerland

17:20 (A-2-3) **Comparative Sensitivity Analysis of High-speed Communication Cores on Flash-based FPGAs**
Morgana Duni, Giorgio Cora, Corrado De Sio, Sarah Azimi, Luca Sterpone
Politecnico di Torino, Italy

17:40 (A-2-4) **Comparing the Severity of the Environmental Tests across Standards**

Donggeun Lee[1], H-J. Park[2], S-I. Sung[1]
[1]*Kyonggi University, South Korea;* [2]*LIG Nex1 Co., South Korea*

Session B-1: Reliability for Nanoelectronics (Cryogenic Temperatures)

Chairs: Michael Waltl, *Institute for Microelectronics, TU Wien, Austria*
Alexander Grill, *imec, Belgium*
Katja Waschneck, *Infineon Technologies, Germany*

Schedule: *Tuesday, 22 September 2026*
11:00 – 13:40

Room: *Graz Room (EI9)*

11:00 (INV-2) **Cryogenic Low-Noise Amplifiers for Quantum Computing: Engineering Noise and Thermal Properties**
Cezar Zota
IBM Research Europe, Switzerland

11:40 (B-1-1) **Hot-carrier Degradation Sense Effect at Cryogenic Temperature in 28NM FD-SOI Transistor**
Goran Durand[1], Mikaël Cassé[2], Xavier Federspiel[1], Philippe Galy[1], Emmanuel Vincent[1], Irina Ionica[3]
[1] *STMicroelectronics, France;* [2] *CEA, France;* [3] *CROMA, France*

12:00 (B-1-2) **Hot-Carrier Reliability of LDMOS Devices at Deep-Cryogenic Temperatures**
Jonas Peis[1], Florian Seilmeier[1], Marc Strasser[1], Amelie Hagelauer[2]
[1] *Infineon Technologies AG, Germany;* [2] *Fraunhofer Institute for Electronic Microsystems and Solid State Technologies EMFT, Germany*

13:20 (B-1-3) **Multi-Regime Trap Dynamics in Si/SiGe/Si MOSFET Current Transients at Cryogenic Temperatures**

Felix Stampfl[1], Bram Veryser[2], Clement Godfrin[2], Bart Raes[2], Sylvain Baudot[2], Yosuke Shimura[2], Kristiaan De Greve[2], Alexander Grill[2], Michael Waltl[1]

[1] *Institute for Microelectronics, TU Wien, Vienna, Austria;* [2] *imec, Leuven, Belgium*

Session B-2

Session B-2: Reliability for Nanoelectronics (Trap Physics, Low-Frequency Noise, and Reliability Modeling)

Chairs: Michael Waltl, *Institute for Microelectronics, TU Wien, Austria*
Alexander Grill, *imec, Belgium*
Katja Waschneck, *Infineon Technologies, Germany*

Schedule: *Tuesday, 22 September 2026*
13:40 – 16:40

Room: *Graz Room (El9)*

13:40 (B-2-1) **PSD-Based Low-Frequency Noise Characterization of FDSOI MOSFETs using a Low-Noise Measurement Setup: Impact of Setup-Induced Distortions**
Paul Sommerer[1], Patrick Reisinger[1], Florian Wimmer[1], Bernhard Stampfer[1], Luca Pirro[2], Markus Kollarik[1], Michael Waltl[1]
[1] *Institute for Microelectronics, TU Wien, Vienna, Austria;* [2] *Globalfoundries, Germany*

14:00 (B-2-2) **Statistical Extraction of Trap Parameters Using Array Test Chips to Study the Impact of Defects on Transistor Technologies**
Martin E. M. Loesener[1], Florian Wimmer[2], Roberto Lacerda de Orio[2], Walter Pflanzl[1], Thomas Fröhlich[1], Rainer Minixhofer[1], Dominic Waldhör[2], Tibor Grasser[2], Michael Waltl[3]
[1] *ams-OSRAM AG, Austria;* [2] *Institute for Microelectronics, TU Wien, Vienna, Austria;* [3] *Christian Doppler Laboratory for Single-Defect Spectroscopy at the Institute for Microelectronics, TU Wien, Austria*

14:20 (B-2-3) **Statistical Study of Low-Frequency Noise in NLA-Processed FDSOI nMOS Transistors**
Patrick Reisinger[1], Florian Wimmer[1], Daphnée Bosch[2], Antoine Albouy[2], Xavier Garros[2], Perrine Batude[2], Tibor Grasser[1], Michael Waltl[1]
[1] *Institute for Microelectronics, TU Wien, Vienna, Austria;* [2] *CEA Leti, France*

14:40 (B-2-4) **Compact Physics-Based SPICE Framework for Reliability-Aware Circuit Simulation (COSMIC)**
Josef Salzmann, Tibor Grasser, Michael Waltl
Institute for Microelectronics, TU Wien, Vienna, Austria

15:40 (B-2-5) **Modeling the nitridation-related TAT (trap-assisted tunneling) in advanced high-k/metal gate transistors**
Elhadji Alhousseyni Diallo, Tadeu Mota Frutuoso, William Vandendaele, Remy Gassilloud, Marie-Claire Cyrille, Claire Fenouillet-Beranger, Xavier Garros
Univ. Grenoble Alpes, CEA, Leti, France

16:00 (B-2-6) **Stacked two-dimensional complementary field effect transistors**
Pranavram Venkatram
Pennsylvania State University, United States

16:20 (B-2-7) **Integration of high-κ gate dielectrics with 2D semiconductors via self-oxidizing vdW metal seed-layers**
Krishnendu Mukhopadhyay, Saptarshi Das
Penn State, United States

Session B-3

Session B-3: Reliability for Nanoelectronics (Memory and Interconnect Technologies)

Chairs: Michael Waltl, *Institute for Microelectronics, TU Wien, Austria*
Alexander Grill, *imec, Belgium*
Katja Waschneck, *Infineon Technologies, Germany*

Schedule: *Thursday, 24 September 2026*
10:20 – 12:00

Room: *Vienna Room (EI7)*

10:20 (INV-8) **Reaching the BTI 10yrs Lifetime for 2.5V BEOL Compatible (<420°C) High Voltage Si-CMOS**
William Vandendaele
CEA-Leti

10:40 (B-3-1) **Noise Spectroscopy of Defects in MIM Capacitors**
Nishant Saini[1], Davide Tierno[2], Kristof Croes[1], Valeri Afanas'Ev[1], Jan Van Houdt[1]
[1] *imec & KU Leuven, Belgium;* [2] *imec, Belgium*

11:00 (B-3-2) **Changes in lines under test containing artificially generated voids in molybdenum implanted molybdenum disilicide due to electromigration**
Julia Baldauf
CiS Forschungsinstitut für Mikrosensorik GmbH, Germany

11:20 (B-3-3) **Reliability of Ge-rich GeSbTe Stack Scaling in Phase-Change Memory**
Jean Rottner, Quy-Khanh Nguyen, Guillaume Bourgeois, Antoine Salvi, Sylvain Gout, Kévin Guy, Leila Fellouh-Boutata, Mathieu Bernard, Simon Martin, Niccolo Castellani, Gabriele Navarro
Univ. Grenoble Alpes, CEA, Leti, F-38000 Grenoble, France

11:40 (B-3-4) **Electrical failure due to Adjacent word-line in H-passivated DRAM and characterization thereof**
Woosic Kim, Daeun Choi, Kyunghwan Kim, Gijong Sung, Daesun Kim, Incheol Nam, Heeil Hong, Sangjun Hwang
Samsung Electronics, South Korea

Session C-1

Session C-1: Progress in Failure Analysis: Defect Detection and Analysis (Sample preparation and Package Level FA)

Chairs: Giovanna Mura, *DIEE University of Cagliari, Italy*
Samuel Chef, *Temasek Laboratories NTU, Singapore*
Christian Hobert, *Sector Technologies SAS, France*

Schedule: *Tuesday, 22 September 2026*
16:40 – 18:00

Room: *Graz Room (El9)*

16:40 (C-1-1) **High-Sensitivity Detection of Microdefects in Scanning Acoustic Tomography Using Neighboring Waveform Integration and Local Contrast Normalization**
Koki Rikimaru[1], Kenji Yasui[1], Kaoru Sakai[1], Masayuki Kobayashi[2], Kotaro Kikukawa[2], Shigeru Ohno[2]
[1] *Hitachi, Ltd., Japan;* [2] *Hitachi Power Solutions Co., Ltd., Japan*

17:00 (C-1-2) **Beyond Defect Detection: Using Scanning Acoustic Microscopy (SAM) to Measure Subsurface Warpage in Flip-Chip Packages**
Marcelo Gomes Abrantes[1], Jeffrey Gutierrez[2], Ugo Raia[2], Kim Baumans[2], Piet De Pauw[2], Houman Zahedmanesh[1]
[1] *IMEC, Faculty of Engineering Sciences (KU Leuven), Belgium;* [2] *IMEC, Belgium*

17:20 (C-1-3) **Submicron Multimodal Infrared Microscopy for Fast Localization and Identification of Sub-10 µm Contamination in Electronic Devices**
Carolin Borbeck[1], Miriam Unger[1], Eoghan Dillon[2], Mustafa Kansiz[2], Michael K. F. Lo[2]
[1] *Photothermal Spectroscopy Corp GmbH, Germany;* [2] *Photothermal Spectroscopy Corp, United States*

17:40 (C-1-4) **Adaptive Laser Ablation with Real-Time Depth and Material Sensing for Failure Analysis Sample Preparation**

Oytun Tasgit, Claudia Radelow, Julia Keller, Henry Spott
3D-Micromac AG, Germany

Session C-2

Session C-2: Progress in Failure Analysis: Defect Detection and Analysis (Defect Localization and Physical Analysis)

Chairs: Samuel Chef, *Temasek Laboratories NTU, Singapore*
Christian Hobert, *Sector Technologies SAS, France*

Schedule: *Wednesday, 23 September 2026*
16:00 – 18:00

Room: *Linz Room (EI10)*

16:00 (INV-7) **Active Auto Thinning (AAT): An AI-Driven Autonomous FIB Endpointing Method Based on Cut-Face Probability Inference and Image Interpolation for Advanced Memory Devices (Best Outstanding Paper Award at ISTFA 2025)**
Bryan Sang Hoon Lee
Micron Technology, USA

16:20 (C-2-1) **Addressing Calibration Instabilities in Thermoreflectance Mapping of IGBT Metallization Using Physically-Constrained Reconstruction**
Mamadou Sanogo[1], Zoubir Khatir[1], Thierry Kociniewski[2]
[1]*UGE- SATIE, France;* [2]*UVSQ - GEMaC, France*

16:40 (C-2-2) **Edge-Induced Current Crowding and Joule Heating–Driven Degradation in Hydrogen-Ion-Modulated Oxide Memory Devices**
Hee Yeon Noh[1], Haripriya G. R.[2], Myoung-Jae Lee[1], Hyeon-Jun Lee[1]
[1]*DGIST, South Korea;* [2]*DGIST, South Korea*

17:00 (C-2-3) **Electrical Open Localization with Quantum Diamond Microscopy**

Christian Herpers[1], Claudia Hobelsberger[1], Max Gert Richter[2], Nicola Kovac[3], Carla Moran Guizan[1], Tobias Zweifel[1], Dominik Muß[1], Daniela Zahn[1], Amelie Hagelauer[4]

[1]*Fraunhofer EMFT Institute for Electronic Microsystems and Solid State Technologies, Germany;* [2]*School of Natural Sciences, Department of Chemistry, Technical University of Munich, Germany;* [3]*Fakultät für Elektrische Energiesysteme & Informationstechnik, Universität der Bundeswehr München, Germany;* [4]*Chair of Micro- and Nanosystems Technology, Technical University of Munich, Germany*

17:20 (C-2-4) **Microstructural Characterization for the Interface of Cu Plated SiO2 Substrate Prepared Using the TORIZING Process by Scanning Transmission Electron Microscopy and Time-of-Flight Secondary Ion Mass Spectrometry**

Masahiko Nishijima[1], Ming-Chun Hsieh[2], Sangmin Lee[3], Takuya Nakagiri[4], Rieko Okumura[1], Chuantong Chen[5], Junji Yoshikawa[6], Yuhei Kitahara[6], Kimihiro Yamanaka[4], Katsuaki Suganuma[4]

[1]*Flexible 3D System Integration Lab, SANKEN, Osaka University, Japan;* [2]*F3D, Sanken, The University of Osaka, Ibaraki, Osaka, Japan;* [3]*F3D, Sanken, The University of Osaka, Ibaraki, Osaka, Japan;* [4]*F3D, Sanken, The University of Osaka, Ibaraki, Osaka, Japan;* [5]*F3D, Sanken, The University of Osaka, Ibaraki, Osaka, Japan;* [6]*Okuno Chemical Co., Ltd, Osaka, Japan*

17:40 (C-2-5) **Thermo-reflectance monitoring in laser voltage imaging for effective bridge defects localization**

Angelo Antonio Merassi

STMicroelectronics, Italy

Session D

Session D: Reliability of Microwave Devices and Circuits

Chairs: Matteo Meneghini, *University of Padova, Italy*
Valeria Rustichelli, *IRT Saint Exupery, France*
David Trémouilles, *LAAS-CNRS, France*

Schedule: *Tuesday, 22 September 2026*
14:40 – 15:00

Room: *Vienna Room (EI7)*

14:40 (F2-1-7) **Impact of the Kink Effect on the Dynamic Large-Signal Performance of GaN HEMTs**
Qingyang Dong, Nuo Li, Ke Wei, Weijun Luo
Institute of Microelectronics, Chinese Academy of Sciences, China

Note: Due to the limited number of submissions in this session, this paper has been integrated into Session F2-1.

Session E-1

Session E-1: Packaging and Assembly Reliability and Failure Analysis (Health Monitoring and Chip Package Interaction)

Chairs: Paolo Cova, *University of Parma, Italy*
Olaf Wittler, *Fraunhofer, Germany*

Schedule: *Wednesday, 23 September 2026*
10:20 – 12:20

Room: *Graz Room (EI9)*

10:20 (E-1-1) **Utilizing Emitter Resistance for Online Condition Monitoring of an IGBT Module**
Narender Lakshmanan[1], James Abuogo[2], Thomas Radke[1], Jörg Franke[2], Josef Lutz[2], Thomas Basler[2]
[1] *Mitsubishi Electric Europe B.V., Ratingen, Germany;* [2] *Chemnitz University of Technology, Chemnitz, Germany*

10:40 (E-1-2) **Exceptional reliability of low-stress direct-cooling intelligent power modules with enhanced manufacturing flexibility**
Byeongchan Kim, Seongkwon Chu, Dongjin Kim
Korea Institute of Industrial Technology, South Korea

11:00 (E-1-3) **Impact of Package Geometry and PCB Constraints on Drift of Bandgap Voltage Reference Circuits during Thermal Aging**
Edinso Gabriel Marina Alonzo[1], René Theodora Hubertus Rongen[2], Michiel van Soestbergen[2], Pierre Turpin[3], Patrick Tounsi[4], Sonia Ben-Dhia[4]
[1] *NXP Semiconductors / Institut National des Sciences Appliquées (INSA), France;* [2] *NXP Semiconductors, Netherlands;* [3] *NXP Semiconductors, France;* [4] *Institut National des Sciences Appliquées (INSA), France*

11:20 (E-1-4) **Aging Assessment of Thermally Regulated LFP Prismatic Cells Using DCIR and EIS Measurements**

Marco Simonazzi, Andrea Toscani, Nicola Delmonte, Valentina Bianchi, Ilaria De Munari, Giovanni Chiorboli, Paolo Cova, Danilo Santoro

University of Parma, Department of Engineering and Architecture, Italy

11:40 (E-1-5) **Integrating GaAs Optical Probes with Power Cycling: In-Gel Tj Sensing and Zth Monitoring**

Danilo Santoro[1], Maryan Zino[2], Md Iftadul Islam Sakib[2], Sachin Kumar Bhoi[2], Gamze Egin Martin[2], Sajib Chakraborty[2], Paolo Cova[1], Nicola Delmonte[1], Omar Hegazy[2]

[1] *University of Parma, Department of Engineering and Architecture, Italy;* [2] *Vrije Universiteit Brussel (VUB), ETEC Department, Belgium*

12:00 (E-1-6) **SAC Soldered Clips vs. DTS: A Clash of Failure Mechanisms and Current-Carrying Capacity**

Knud Gripp[1], Jesco Beyer[1], Aylin Behrendt-Bicakci[2], Benjamin Fabian[3], Frank Krüger[3], Christian Kersting[3], Anton-Zoran Miric[3]

[1] *HAW Kiel; FuE GmbH, Germany;* [2] *HAW Kiel, Germany;* [3] *Heraeus Electronics GmbH & Co. KG, Germany*

Session E-2

Session E-2: Packaging and Assembly Reliability and Failure Analysis (Reliability and Characterisation of Packaging Materials)

Chairs: Kirsten Weide-Zaage, *RESRI IMS Leibniz Universität Hannover, Germany*

Schedule: *Wednesday, 23 September 2026*
13:20 – 16:40

Room: *Graz Room (EI9)*

13:20 (INV-6) **Ultra-Reliable All-Liquid Interconnections for Power Electronics Components**
Francesco Iannuzzo
Polytechnic of Turin, Italy

14:00 (E-2-1) **Mechanical Stress Modulates Surface-Diffusion-Driven Morphology Changes in Subtractive Ru Nano-Interconnects**
Houman Zahedmanesh[1], Gilles Delie[2], Myriam Vander Peer[2], Hajdin Ceric[3], Ahmed Saleh[2], Marta Agati[2], Chen Wu[2], Seongho Park[2]
[1] *imec, KU Leuven, Belgium;* [2] *imec, Belgium;* [3] *Institute for Microelectronics, TU Wien, Vienna, Austria*

14:20 (E-2-2) **Reliability Testing of SMDs Using an Accelerated Mechanical Shear Fatigue Approach**
Bernhard Czerny[1], Thomas Walter[2], Moritz Hartleb[2], Martin Kern[3], Niklas Grill[3], Golta Khatibi[4]
[1] *University of Applied Sciences Burgenland, Austria;* [2] *TU Wien, Austria;* [3] *Forschung Burgenland, Austria;* [4] *Institute of Chemical Technologies and Analytics, TU Wien, Austria*

14:40 (E-2-3) **Corrosion-Induced Crack Formation in AlN AMB Substrates under Temperature Humidity Bias Conditions**
Ralf Schmidt, Michael Endres, Robert Gospos, Patrick Dreher, Martin Neumann
SIEMENS AG, Germany

15:00 (E-2-4) **Chip-Scale Interfacial Fracture Evaluation of Glass/Cu Metallization Using a Modified Four-Point Bending test**
Seungmin Cho[1], Sangmin Lee[1], Minseo Kim[1], Masahiko Nishijima[1], Aiji Suetake[1], Junji Yoshikawa[2], Yuhei Kitahara[2], Chuantong Chen[1], Takuya Nakagiri[1], Ming-Chun Hsieh[1], Kimihiro Yamanaka[1], Katsuaki Suganuma[1]
[1]*F3D, Sanken, The University of Osaka, Ibaraki, Osaka, Japan;* [2]*Okuno Chemical Co., Ltd, Osaka, Japan*

16:00 (E-2-5) **Individual Effect of Organic Electroplating Additives on Cu-Sn Degradation in Flip Chip Packaging**
Jasper Coppen[1], Fatin Battal[2], Greta Terzariol[3], Amar Mavinkurve[3], Willem Van Driel[1], Yaiza Gonzalez-Garcia[1], Arjan Mol[1]
[1]*Delft University of Technology, Netherlands;* [2]*Radboud University, Netherlands;* [3]*NXP Semiconductors, Netherlands*

16:20 (E-2-6) **Microstructural evolution of thick ultrasonic bonded copper wires**
Liz Karanja[1], Pierre-Yves Pichon[2], Marc Legros[1]
[1]*CEMES-CNRS, France;* [2]*Mitsubishi Electric R&D Centre Europe, France*

Session F1

Session F1: Power Devices Reliability: Smart-Power Devices and Silicon Power Devices (Reliability of Power Devices and Related Materials)

Chairs: Michael Nelhiebel, *Infineon/KAI, Austria*
Thomas Basler, *TU Chemnitz, Germany*

Schedule: *Wednesday, 23 September 2026*
16:00 – 18:00

Room: *Vienna Room (EI7)*

16:00 (F1-1) **Evolution of inter and intragranular microstructure of Cu films and interconnects during in situ TEM heating cycles.**
Liz Karanja[1], Sebastian Moser[2], Michael Reisinger[2], Marc Legros[1]
[1]*CEMES-CNRS, France;* [2]*KAI Kompetenzzentrum Automobil und Industrieelektronik GmbH, Villach, Austria*

16:20 (F1-2) **Applicability of Charge Pumping in Measure-Stress-Measure Schemes for the Investigation of Trench-MOSFET Avalanche Degradation**
Keanu Zenz[1], Gregor Pobegen[1], Florian Rigaud-Minet[2], Andrew Wood[2], Michael Waltl[3]
[1]*KAI - Kompetenzzentrum Automobil- und Industrieelektronik GmbH, Austria;* [2]*Infineon Technologies AG, Austria;* [3]*Institute for Microelectronics, TU Wien, Vienna, Austria*

16:40 (F1-3) **Investigation of Chip Bending Strain and Polyimide Delamination around Gate-Finger and Gate-Ring Regions in SiC MOSFETs under Short-Circuit Conditions Using a 2D Multiphysics FEM with Cohesive Zone Modelling**
Mustafa Shqair, Emmanuel Sarraute, Frédéric Richardeau
LAPLACE, Université de Toulouse, Toulouse INP, CNRS, France

17:00 (F1-4) **Sub-grain-resolved Analysis of Degradation in Cu Metallization via Scanning 3DXRD and Thermomechanical Modeling**

Nikhil Prabhu[1], Laura Neumann[2], Michael Reisinger[3], James Ball[4], Cedric Corley-Wiciak[4], Manuel Petersmann[3], Agnieszka Corley-Wiciak[4], Carsten Detlefs[4], Jon Wright[4], Martin Diehl[1]

[1] *KU Leuven, Belgium;* [2] *Fraunhofer IKTS, Germany;* [3] *KAI GmbH, Austria;* [4] *ESRF, France*

17:20 (F1-5) **Low-Cost Micro-Sized Ag–Si Composite Paste Sintering and Structural Reliability Analysis for SiC Power Modules**

Chuantong Chen[1], Yang Liu[1], Minoru Ueshima[2], Masahiko Nishijima[1], Sangmin Lee[1], Katsuaki Suganuma[1]

[1] *The University of Osaka, Japan;* [2] *Daicel Corporation, Japan*

17:40 (F1-6) **TDDB in polymer-based galvanic isolators under asymmetric voltage waveforms: insights into the role of electromechanical stress**

Gabriele Scarpiello[1], Matteo Greatti[1], Tarundeep Singh[1], Dario Paci[2], Donata Asnaghi[3], Francesco Guzzi[2], Marco Salina[3], Fabrizio Speroni[2], Michele Lauria[3], Vincenzo Marano[3], Alessandro Sottocornola Spinelli[1], Christian Monzio Compagnoni[1], Gerardo Malavena[1]

[1] *Politecnico di Milano - Dipartimento di Elettronica, Informazione e Bioingegneria (DEIB), Italy;* [2] *STMicroelectronics, 20007 Cornaredo, Italy;* [3] *STMicroelectronics, 20864 Agrate Brianza, Italy*

Session F2-1

Session F2-1: Power Devices Reliability: Wide-Bandgap Devices (SiC Power Devices)

Chairs: Matteo Meneghini, *University of Padova, Italy*
Valeria Rustichelli, *IRT Saint Exupery, France*
David Trémouilles, *LAAS-CNRS, France*

Schedule: *Tuesday, 22 September 2026*
11:00 – 15:00

Room: *Vienna Room (EI7)*

11:00 (INV-1) **Enabling Large Scale Implementation of Reliable WBG Devices from a Manufacturer's Viewpoint**
Stefano Aresu
Infineon Technologies, Austria

11:40 (F2-1-1) **Influence of High-Side Component and Intrinsic Parameters on SiC MOSFET Switching Dynamics Using Double Pulse Test**
Thierno Abass Diallo[1], Laurent Dupont[2], Stéphane Lefebvre[3], Jean-Pierre Fradin[4], Joao Oliveira[5], Michel Piton[6]
[1]*ENS Paris-Saclay, France;* [2]*Université Gustave Eiffel, France;* [3]*CNAM Paris, France;* [4]*ICAM Toulouse, France;* [5]*IRT Saint-Exupéry, France;* [6]*ALSTOM, France*

12:00 (F2-1-2) **Dynamic Current Balancing of Paralleled Trench SiC-Mosfet Devices Using Fully Digital Feedback Control**
Ravi Nath Tripathi, Ichiro Omura
Kyushu Institute of Technology, Japan

13:20 (F2-1-3) **Carrier Lifetime Analysis on SiC Devices Using Open-Circuit Voltage Decay: Insight to Suppress Bipolar Degradation**
Hiroaki Matsumori[1], Wataru Shimmi[1], Hitoshi Sakane[1], Masashi Kato[1]
[1]*Nagoya Institute of Technology, Japan*

13:40 (F2-1-4) **Threshold Voltage Instability in State-of-the-Art SiC Transistors: Experimental Analysis and Challenges**
Giorgio Zappalà[1], Daniele Lideo[1], Carlo De Santi[1], Gaudenzio Meneghesso[1], Enrico Zanoni[1], Matteo Meneghini[1]
[1]*University of Padova, Italy*

14:00 (F2-1-5) **Gate Switching Stress Induced Hysteresis Modification of Silicon Carbide MOSFETs: Implication for Bias Dependent Trap Dynamics**
Sven Thiele[1], Venkata Shanmukha Srivatsav Pakki[1], Holger Heinisch[2], Thomas Basler[1]
[1]*Chair of Power Electronics, Chemnitz University of Technology, Germany;* [2]*Engineering Power Components, Robert Bosch GmbH, Germany*

14:20 (F2-1-6) **Preconditioned BTI measurement with arbitrary gate preconditioning: A gated-diode-free readout for SiC MOSFETs**
Johannes Kügler[1], Fabian Rasinger[2], Aleksey Mikhaylov[2], Gregor Pobegen[1]
[1]*KAI GmbH, Austria;* [2]*Infineon Technologies Austria AG, Austria*

14:40 (F2-1-7) **Impact of the Kink Effect on the Dynamic Large-Signal Performance of GaN HEMTs**
Qingyang Dong, Nuo Li, Ke Wei, Weijun Luo
Institute of Microelectronics, Chinese Academy of Sciences, China

Session F2-2: Power Devices Reliability: Wide-Bandgap Devices (GaN Power Devices)

Chairs: Matteo Meneghini, *University of Padova, Italy*
Valeria Rustichelli, *IRT Saint Exupery, France*
David Trémouilles, *LAAS-CNRS, France*

Schedule: *Wednesday, 23 September 2026*
10:20 – 12:20

Room: *Vienna Room (EI7)*

10:20 (F2-2-1) **H-terminated Vertical GaN Diodes Under Electrical Stress: Characterization and Modeling**
Ambra Maria Vianello[1], Simone Leonardo Longato[1], Manuel Fregolent[1], Fabiana Rampazzo[1], Matteo Buffolo[2], Dawei Wang[3], Bingcheng Da[3], Houqiang Fu[3], Shisong Lou[4], Cheng Chang[4], Yuji Zhao[4], Isabella Rossetto[1], Carlo De Santi[1], Gaudenzio Meneghesso[1], Enrico Zanoni[1], Matteo Meneghini[2]
[1]*Department of Information Engineering, University of Padua, Italy;* [2]*Department of Information Engineering, University of Padua, Italy;* [3]*School of Electrical, Computer, Energy Engineering, Arizona State University, Tempe, AZ, USA;* [4]*Department of Electrical and Computer Engineering, Rice University, Houston, TX, USA*

10:40 (F2-2-2) **Failure mechanisms of Schottky-Gate p-GaN HEMTs in Gate Reliability investigation**
Alessio Pirani, Alberto Millefanti, Andrea Olietti, Lorenzo Cerati, Viviana Fezzi, Cristina Miccoli, Ferdinando Iucolano, Giansalvo Pizzo
STMicroelectronics, Italy

11:00 (F2-2-3) **Improvement of GaN HEMT Reliability by Reduction of Intrinsic Oxygen**

Benjamin Weber[1], Michael Dammann[1], Peter Brückner[1], Martina Baeumler[1], Andreas Graff[2], Michel Simon-Najasek[2], Philipp Neininger[1], Rüdiger Quay[1]

[1]*Fraunhofer IAF, Germany;* [2]*Fraunhofer IMWS, Germany*

11:20 (F2-2-4) **Threshold Voltage Instability in Schottky p-GaN Gate HEMTs Under Dynamic Gate Stress**

Maurizio Millesimo[1], Angela Terracina[2], Santina Bevilacqua[2], Valeria Rustichelli[3], Alfio Russo[2], Claudio Fiegna[1], Andrea Natale Tallarico[1]

[1]*ARCES-DEI, University of Bologna, Italy;* [2]*STMicroelectronics, Italy;* [3]*IRT Saint Exupéry, France*

11:40 (F2-2-5) **Spatio-Temporal Strain-Imaging of Switching in GaN/Si High Electron Mobility Transistors**

Cedric Corley-Wiciak[1], Nicolas Til Sammler[2], Boris Butej[2], Manuel Petersmann[2], Agnieszka Corley-Wiciak[1], Laura Neumann[3], Juan-Manuel Carrillo-Larrea[1], Paul Schmiedeke[4], Marc Strätgen[5], Paul Antoine Douissard[1], Steven J. Leake[1], Peter Boesecke[1], Markus Sievers[6], Michael Glavanovics[6], Dionyz Pogany[7], Michael Reisinger[6], Tobias Schulli[1]

[1]*ESRF - European Synchrotron Radiation Facility, France;* [2]*KAI GmbH - Kompetenzzentrum Automobil- und Industrieelektronik, Austria;* [3]*Fraunhofer IKTS, Germany;* [4]*Infineon Technologies AG, Germany;* [5]*Infineon Technologies Austria AG, Austria;* [6]*KAI GmbH - Kompetenzzentrum Automobil- und Industrieelektronik, Austria;* [7]*Institute of Solid State Electronics, TU Wien, Austria*

12:00 (F2-2-6) **Radiative Recombination in p-GaN Gate HEMTs: The Role of an AlGaN Back-Barrier**

Roland Strieder[1], Rajarshi Roy Chaudhuri[2], Boris Butej[3], Manuel Stabentheiner[4], Joao Lucas Gomes[4], Christian Koller[4], Clemens Ostermaier[4], Dionyz Pogany[5], Michael Waltl[2]

[1]*Wolfgang Pauli Institute, Vienna, Austria;* [2]*Institute for Microelectronics, TU Wien, Vienna, Austria;* [3]*KAI GmbH, Austria;* [4]*Infineon Technologies Austria AG, Austria;* [5]*TU Wien, Vienna, Austria*

Session F2-3

Session F2-3: Power Devices Reliability: Wide-Bandgap Devices (GaN and SiC Power Devices)

Chairs: Matteo Meneghini, *University of Padova, Italy*
Valeria Rustichelli, *IRT Saint Exupery, France*
David Trémouilles, *LAAS-CNRS, France*

Schedule: *Wednesday, 23 September 2026*
13:20 – 15:20

Room: *Vienna Room (EI7)*

13:20 (F2-3-1) **Investigation of Planar Gate-Oxide Active Electron Detrapping for On-Line VGS(TH) Drift Compensation Using an X-Level Gate-Driver Topology in SiC MOSFET Phase-Leg under PWM Operation**

Frédéric Richardeau[1], Mathis Picot-Digoix[1], Camille Bidaud[2], Jean-Marc Blaquière[1], Sébastien Vinnac[1], Stéphane Azzopardi[3], Long Thanh Le[3]

[1]*LAPLACE, Université de Toulouse, Toulouse INP, CNRS, France;* [2]*Safran Tech Paris-Saclay - LAPLACE, Université de Toulouse, Toulouse INP, CNRS, France;* [3]*Safran Tech Paris-Saclay, France*

13:40 (F2-3-2) **Impact of High Gate-Bias Stress on Interface Trap Density and Reverse Conduction in SiC Planar MOSFETs**

Yu-Cheng Wang[1], Yen-Chun Lin[1], Prasannajeet Singh[2], Tsung-Yu Yu[1], Hsin-Chieh Liang[1], Pei-Tien Chen[2], Yi-Kai Hsiao[3], Yogesh Singh Chuahan[4], Hao-Chung Kuo[2], Tian-Li Wu[2], Chang-Ching Tu[2]

[1]*National Central University, Taiwan;* [2]*National Yang Ming Chiao Tung University, Taiwan;* [3]*Hon Hai Research Institute, Taiwan;* [4]*India Institute of Technology Kanpur, India*

14:00 (F2-3-3) **Exponential and Logarithmic Recovery Dynamics in GaN GITs Subjected to Hot-Carrier Stress**

Nicolas Til Sammler[1], Boris Butej[1], Gregor Pobegen[1], Christian Koller[2], Clemens Ostermaier[2], Dionyz Pogany[3]

[1]*KAI GmbH - Kompetenzzentrum Automobil- und Industrieelektronik, Austria;* [2]*Infineon Technologies Austria AG;* [3]*Institute of Solid State Electronics, TU Wien, Austria*

14:20 (F2-3-4) **Fowler Nordheim Correction of Gate Oxide Thickness for TDDB Lifetime Measurement Improvement.**

Marco Finocchiaro, Leonardo Gervasi, Alfio Russo, Erwin Schroer

STMicroelectronics, Italy

14:40 (F2-3-5) **Single-Pulse Short-Circuit Ruggedness and Bias-Induced Oscillatory Behavior in latest-generation Commercial 650V p-GaN Schottky Gate GaN HEMTs**

Kulisa Nanayakkara[1], Keiji Watanabe[2], Shuji Endo[2], Motoo Matsushita[2], Matoba Hirotsugu[3], Shinichi Domae[3], Alberto Castellazzi[1]

[1]*Solid-State Power Processing Laboratory, Kyoto University of Advanced Science, Japan;* [2]*Automotive Motor & Electronic Control Business Unit , Nidec Corporation, Japan;* [3]*Nagamori Institute of Actuators , Kyoto University of Advanced Science, Japan*

15:00 (F2-3-6) **Threshold Voltage Instability in SiC MOSFET, Cascode GaN, and p-GaN HEMT Under MHz Gate Switching Stress**

Rustam Kumar, Carlo De Santi, Gaudenzio Meneghesso, Enrico Zanoni, Matteo Meneghini

University of Padova, Padova, Italy

Session F3

Session F3: Power Devices Reliability: Power Electronic Systems

Chair: Omar Hegazy, *Vrije Universiteit Brussel, Belgium*

Schedule: *Tuesday, 22 September 2026*
15:40 – 17:40

Room: *Vienna Room (EI7)*

15:40 (F3-1) **Investigation into the Dynamic Shift of Zero-Temperature Coefficient Considering On-Resistance in SiC MOSFETs at Low Gate Voltages**
Zeng Xuan[1], Xiaohui Xu[2], Jingyang Hu[3], Ying Zhao[2], Mengfei Xu[2], Yujie Zhao[3], Haoze Luo[3], Xiangning He[3]
[1]*College of Integrated Circuits Zhejiang University, China;* [2]*Wuhan Institute of Marine Electric Propulsion, China;* [3]*College of Electrical Engineering Zhejiang University, China*

16:00 (F3-2) **Non-Invasive Diagnosis of Localized Aging in VSC-HVDC DC-Link Capacitors via Differential Harmonic Impedance**
Yong Yang[1], Jiajie Song[1], Yi Liu[2]
[1]*State Grid Economic and Technological Research Institute Co., Ltd., China;* [2]*Tiangong University, China*

16:20 (F3-3) **Comparison of Two Multi-functional X-Level Gate-Drivers for Enhancing SiC MOSFET Short-Circuit Resilience and EMI Compliance**
Camille Bidaud[1], Frédéric Richardeau[2], Mathis Picot-Digoix[1], Jean-Marc Blaquiere[2], Sébastien Vinnac[2], Emmanuel Sarraute[2], Stéphane Azzopardi[1], Thanh-Long Le[1]
[1]*SAFRAN TECH, Paris - Saclay, France;* [2]*LAPLACE, University of Toulouse, CNRS, INPT, France*

16:40 (F3-4) **Characterization of On-State Voltage Measurement Circuits for Bidirectional Wide-Bandgap Semiconductors**

Karla Draženović[1], Marinko Kovačić[1], Michael Glavanovics[2]

[1] *University of Zagreb Faculty of Electrical Engineering and Computing, Croatia;* [2] *Infineon Technologies (KAI), Austria*

17:00 (F3-5) **A Sensor-Physics-Informed Neural Network for Remaining Useful Life Prediction of Aluminum Electrolytic Capacitors**

Yi Liu[1], Zhiqiang Liu[2], Yao Ma[1], Yunhui Mei[1]

[1] *Tiangong University, China;* [2] *China First Automobile Works Group Co., Ltd., China*

17:20 (F3-6) **Reliability Investigation on High Voltage Power SiC Modules with High-Performance Joining Technology**

Lukas Hein[1], Thomas Basler[1], Tobias N. Wassermann[2], Anton Rossin[2]

[1] *University of Technology Chemnitz, Germany;* [2] *Infineon Technologies AG, Germany*

Session G: Photonics Reliability

Chairs: Yannick Deshayes, *IMS Laboratory, France*
Michel Garcia, *III-V Lab, France*

Schedule: *Wednesday, 23 September 2026*
10:20 – 12:20

Room: *Linz Room (EI10)*

10:20 (INV-5) **From Device Reliability to System Reliability: Challenges Across the Photonics Value Chain**
Michael Rogers
ams OSRAM AG, Austria

11:00 (G-1) **Intrinsic and extrinsic drift of Dark Count Rate in 3D stacked Single-Photon Avalanche Diode (SPAD) after High Temperature Operating Life stress**
Duc Tung Vu[1], Bastien Mamdy[2], Djihad Amina Djemmah[1], Thibauld Cazimajou[3], Patrick Pittet[3], Dominique Golanski[2], Sebastien Place[2], Isobel Nicholson[4], Francis Calmon[1]
[1]*Univ Lyon, INSA Lyon, INL, UMR5270, 69621 Villeurbanne, France;* [2]*STMicroelectronics, 850 rue Jean Monnet, Crolles, France;* [3]*Univ Lyon, Université Claude Bernard Lyon 1, INL, UMR5270, 69622 Villeurbanne, France;* [4]*STMicroelectronics, 1 Tanfield, Inverleith Row, Edinburgh, United Kingdom*

11:20 (G-2) **New strategy for selecting commercial LEDs for space applications**
Augusto Mura[1], Piero Spezzigu[2], Hugo Bourguignon[2], E. Courtade[3], M. Fongral[3], O. Gilard[3], G. Mura[4], Y. Deshayes[1]
[1]*Université de Bordeaux, École Doctorale SPI, IMS, Bordeaux, France;* [2]*Intraspec Technologies, France;* [3]*CNES, France;* [4]*Università degli Studi di Cagliari, Italy*

11:40 (G-3) **Reliability Assessment for InGaAs/InP Multi-cell Single Photon Avalanche Diode (MCSPAD) Integrated with Quenching Resistor**

Heewon Bang[1], Bora Jeon[2], Seungchul Yang[2], Junghyun Kim[2], Ilgu Yun[1]

[1] *Yonsei University, South Korea;* [2] *Wooriro Co., South Korea*

12:00 (G-4) **Modeling and Reliability Tests of 330 nm AlGaN UV-A LED with Tunnel Junction**

Jakub Pacuk[1], Francesco Piva[1], Nicola Roccato[1], Matteo Buffolo[2], Agnes M. D. M. Xavier[3], Andy Allerman[4], Shamsul Arafin[3], Siddharth Rajan[3], Carlo De Santi[1], Nicola Trivellin[5], Gaudenzio Meneghesso[1], Enrico Zanoni[1], Matteo Meneghini[2]

[1] *Department of Information Engineering, University of Padova, Padova, Italy;* [2] *Department of Information Engineering; Department of Physics and Astronomy, University of Padova, Padova, Italy;* [3] *Department of Electrical and Computer Engineering, The Ohio State University, Columbus, USA;* [4] *Sandia National Laboratories, Albuquerque, USA;* [5] *Department of Information Engineering; Department of Industrial Engineering, University of Padova, Padova, Italy*

Session H: MEMS and Sensor Reliability

Chair: Loukas Michalas, *Department of Electrical and Computer Engineering, Democritus University of Thrace, Greece*

Schedule: *Wednesday, 23 September 2026*
13:20 – 15:20

Room: *Linz Room (EI10)*

13:20 (H-1) **Buckling-limited reliability of (Mo, SiNxOy/SiNx) MEMS Micro Hotplates**
Katrin Unger[1], Stefanie Aichhorn[1], Paulina Piller[1], Manu Garg[1], Munir Azeem Syed[1], Andrianov Nikolai[1], Florentyna Sosada-Ludwikowska[2], Larissa Egger[2], Olga Casals[3], Daniel Prades[4], Andreas Tekautz[5], Michael Donnelly[5], Ali Roshanghias[1], Clement Fleury[1]
[1]*Silicon Austria Labs GmbH, 8010 Graz, Austria;* [2]*Materials Center Leoben Forschung GmbH, Vordernberger Straße 12, 8700 Leoben, Austria;* [3]*Universitat de Barcelona, Gran Via De Les Corts Catalanes 585, Barcelona 08007, Spain;* [4]*Universitat de Barcelona, Spain; Technische Universität Braunschweig, 38092 Braunschweig, Germany;* [5]*UnravelTEC OG, 8010 Graz, Austria*

13:40 (H-2) **Electrical Properties of HfO2 thin films for Application in RF-MEMS Capacitive Switch**
Ioannis Kochylas[1], Paolo Martins[2], John Theocharis[1], Doriane Jussey[3], Aymen Mahjoub[4], Etienne Eustache[4], Maria Giannouri[1], Afshin Ziaei[2], George Papaioannou[5]
[1]*National and Kapodistrian University of Athens, Greece;* [2]*Thales Research & Technology, France;* [3]*Thales TRT, France;* [4]*Thales Research and Technology, France;* [5]*University of Athens, Greece*

14:00 (H-3) **Viscoelastic Behaviour of the ADGM1001 RF MEMS Switch Technology**
Russell Duane[1], Ruth Houlihan[1], Brendan Sheehan[1], Padraig Fitzgerald[2], Michael Twohig[2]
[1] *Tyndall National Institute, Ireland;* [2] *Analog Devices International, Limerick, Ireland*

14:20 (H-4) **Electrical, chemical, and structural reliability of HfO2/SiO2 gate-stack ISFETs**
Vladimir Kolkovsky, Eberhard Kurth
Fraunhofer IPMS, Germany

14:40 (H-5) **Exploiting Machine Learning for Assessing the Pull-In Voltage in Bridge Type RF MEMS Capacitive Switches**
Loukas Michalas
Department of Electrical and Computer Engineering, Democritus University of Thrace, Greece

15:00 (H-6) **Effect of the temperature and humidity on quasi-static piezoactuated micromirrors.**
Paola Sabrina Barbato, Christian Verrengia Caporossi, Valeria Casuscelli, Immacolata Pedaci
STMicroelectronics Srl, Italy

Session I

Session I: Extreme environments and Radiation

Chairs: Francesco Pintacuda, *STMicroelectronics, France*

Schedule: *Thursday, 24 September 2026*
10:20 – 12:00

Room: *Graz Room (EI9)*

10:20 (I-1) **Filtered High-Energy X-Ray Generator as an Alternative to Cobalt-60 for Total Ionizing Dose Testing of Electronics**
Guillaume Carpentier[1], Jérôme Boch[2], Frédéric Saigné[2], Tadec Maraine[2], Julien Favrichon[1]
[1] *The French Alternative Energies and Atomic Energy Commission CEA, France;* [2] *University of Montpellier, France*

10:40 (I-2) **A Unified Bulk Electron Mobility Model for 4H-SiC from Cryogenic to High Temperatures**
Giacomo Drudi, Luigi Balestra, Susanna Reggiani
ARCES and DEI, University of Bologna, Bologna, Italy

11:00 (I-3) **TDDB Quantitative Analysis of Heavy-Ion Irradiation Fluence Effects on SiC MOSFET Gate Damage**
Qifei Yuan
China Academy of Space Technology, Beijing, China

11:20 (I-4) **Study of the effects of the gate switch and repetitive short-circuit stress tests on the neutron failure rate of SiC power MOSFETs**
Francesco Pintacuda[1], J. Oliveira[2], O. Perrotin[3], L. Guillot[3], F. Coccetti[2], F. Tilhac[3], C. Cazzaniga[4], M. Kastriotou[4], C. Frost[4], F. Principato[5]
[1] *STMicroelectronics, Italy;* [2] *IRT Saint Exupéry, France;* [3] *ALTER TECHNOLOGY FRANCE, France;* [4] *ISIS Facility, UKRI-STFC, Rutherford Appleton Laboratory, United Kingdom;* [5] *Palermo University, Italy*

11:40 (I-5) **Machine learning approach to predict package dependent parameters of the CDM waveforms**

Leonardo Di Biccari, Paolo Valente, Alessandro Valerio
STMicroelectronics, Italy



Session J

Session J: Automotive and Industrial Electronic Reliability

Chairs: Christoph Hametner, *Institute of Mechanics and Mechatronics, TU Wien, Austria*

Schedule: *Tuesday, 22 September 2026*
13:20 – 14:40

Room: *Villach Room (EI8)*

13:20 (INV-3) **Automotive Battery Management Chipset, In-field, Maintenance & Lifetime**
Wenzel Prochazka
NXP Semicondutors, Austria

14:00 (J-1) **Temperature-dependent calendar aging of Na3V2(PO4)2F3/Hard Carbon Sodium-Ion Batteries: Activation Energy and Degradation Behavior**
Clément Lesage[1], Olivier Briat[2], Jean-Philippe Bellomo[3], Jean-Michel Vinassa[2]
[1]Univ. Bordeaux, CNRS Bordeaux INP, IMS, UMR 5218, F-33400 Talence, France/Alstom Transport SA, F-65600 Séméac, France; [2]Univ. Bordeaux, CNRS Bordeaux INP, IMS, UMR 5218, F-33400 Talence, France; [3]Alstom Transport SA, F-65600 Séméac, France

14:20 (J-2) **A Reliability Spectrum Analysis Method for Vibration Isolator Selection in Automotive Inverters**
Yi Liu, Rui Song, Yunhui Mei
Tiangong University, China

Poster Session

Schedule: *Tuesday, 22 September 2026*
17:40 – 20:00
Room: *Conference Venue*

A-P1	**Steady-state Thermal Modeling Method Considering Thermal Coupling Effect for Power Electronic Equipment** Chunlin Lv, Yichen Xie, Yan Zhang *Xi'an Jiaotong University, China*
A-P2	**A Physics-Informed Gray-Box Model for Multi-Step Forecasting of Transformer Top-Oil Temperature** Yihan Chen[1], Mingyao Ma[1], Wenting Ma[1], Rui Zhang[2] [1]*Hefei University of Technology, China;* [2]*Sungrow Smart Maintenance Technology Co., Ltd, China*
A-P3	**ElectroChemical Migration (ECM) in Harness and Connectors for Harsh environments** Sakthivel Kandasamy *SLB, France*
A-P4	**An Industrial Reliability Evaluation Framework for Capacitors Under Accelerated Aging Tests** Chunlin Lv, Boyang Jin, Pingjunjin Tan, Jinjun Liu *Xi'an Jiaotong University, China*
A-P5	**A reliability optimisation method based on an improved Kriging approximation model** Hao Chen, Shanxue Zhao, Xuerong Ye *Harbin Institute Of Technology, China*

A-P6 **Moisture uptake detection in 3D printed composite materials through relaxation peak tracking Using Impedance spectroscopy**

Anwar Benjana[1], Corinne Dejous[1], Jalal El Yagoubi[2], Isabelle Bord Majek[1]

[1]*Univ. Bordeaux, CNRS, Bordeaux INP, IMS, UMR 5218, F-33400, Talence, France;* [2]*Univ. Bordeaux, CNRS, Bordeaux INP, I2M, UMR 5295, F-33400, Talence, France*

A-P7 **Failure Analysis of Selective Short Circuit in Chip Ceramic Capacitors Influenced by Large Mass Components**

Shuai Wang[1], Meng Cao[1], Xinran Lv[2], Xiaoran Cheng[1], Zhibin Wang[1]

[1]*China Aerospace Components Engineering Center, China;* [2]*Supply Chain Center of China Academy of Space Technology, China*

A-P8 **Avalanche Impedance Measurements on GaN Vertical P-N Diodes and Si Commercial Devices**

Alberto Marcuzzi[1], Carlo De Santi[1], Manuel Fregolent[1], Giacomo Biasin[1], Simone Leonardo Longato[1], Junrui Lyu[2], Allison Brand[2], Mohammed El Amrani[3], Zhengliang Bian[2], Julien Buckley[3], Woong Kwon[4], Hiroshi Amano[5], Gaudenzio Meneghesso[1], Enrico Zanoni[1], Matteo Meneghini[6], Srabanti Chowdhury[2]

[1]*Department of Information Engineering, University of Padova, Italy;* [2]*Department of Electrical Engineering, Stanford University, United States;* [3]*Univ. Grenoble Alpes, CEA, Leti, France;* [4]*(Formerly with) Graduate School of Engineering, Nagoya University, Japan;* [5]*Institute of Materials and Systems for Sustainability (IMASS) and Institute for Advanced Research, Nagoya University, Japan;* [6]*Department of Information Engineering, Department of Physics and Astronomy, University of Padova, Italy*

A-P9 **A Modified Zeller-Based Empirical Method for Cosmic-Ray FIT Estimation for High-Voltage Disk Diodes and Thyristors**

Sajad Ansari, Yangang Wang

Dynex Semiconductor Limited, United Kingdom

A-P10 **Non-destructive detection of counterfeit amplifiers through electrical, thermal and electro-thermal inspection: a comparative study**

Giovanna Mura[1], Francesca Brodu[1], Simone Carta[1]

[1]*DIEE - University of Cagliari, Italy;*

Poster Session

B-P1 **A Meta-study of BTI in GAA nano-sheet technology for reliability prediction**
Mamta Dhyani, Joseph B. Bernstein
Ariel University, Israel

B-P2 **Denoising Strategy for VCM-based ReRAM Devices**
Fabiana Taglietti, Kristoffer Schnieders, Yang Chen, Daniele Storelli, Stefan Wiefels
Peter-Grünberg-Institut 7 (PGI-7), Forschungszentrum Jülich GmbH, Jülich, Germany

B-P3 **Statistical Extraction of Random Telegraph Noise Parameters from Large-Scale N-MOSFET Arrays using Hidden Markov Models**
Tomomi Ishikawa[1], Takuma Hamasaki[2], Akinobu Teramoto[1]
[1]*Research Institute for Semiconductor Engineering, Hiroshima University, Japan;* [2]*Graduate School of Advanced Science and Engineering, Hiroshima University, Japan*

B-P4 **Electromigration reliability modelling: from full-physics to surrogate models for efficient uncertainty quantification**
Ahmed Sobhi Saleh[1], Hajdin Ceric[2], Kristof Croes[1], Robin Callens[3], Ben Van Bavel[3], David Moens[3], Ingrid De Wolf[4], Houman Zahedmanesh[4]
[1]*IMEC, Belgium;* [2]*Institute for Microelectronics, TU Wien, Vienna, Austria;* [3]*KU Leuven, Belgium;* [4]*KU Leuven & IMEC, Belgium*

B-P5 **Influence of single Charge-Trap on Drain Current in nanoscale MOSFET**
Martin Apro, Alicja Michalowska-Forsyth
Graz University of Technology, Institute of Electronics, Austria

B-P6 **Self-Healing in Bi2SeO5-Gated MoS2 FETs: From Counterclockwise Hysteresis to Reversible PBTI**
Jianming Huang, Shaokai Zhou, Hao Li, Haihui Cai, Yury Yurievich Illarionov
L2DON, MSE Department, Southern University of Science and Technology, Shenzhen, China

B-P7 **Optimal Current Regime for Reliable Switching of Perpendicular SOT-MRAM**
Bernhard Pruckner, Viktor Sverdlov, Siegfried Selberherr
Institute for Microelectronics, TU Wien, Vienna, Austria

C-P1 **Alternative physical analysis on 100V p-GaN HEMTS for failure analysis and reliability**
Viviana Fezzi, Francesco Cazzaniga, Andrea Serafini, Alessio Pirani, Giansalvo Pizzo, Alberto Millefanti, Andrea Olietti, Cristina Miccoli
STMicroelectronics, Italy

C-P2 **Research on Leakage Failure Analysis of Supercapacitors Based on Reliability Physics**
Chengcheng Chen, Gang Zhu, Yaru Jiang, Guanghui He, Luo Hongwei
China Electronic Product Reliability and Environment Test Research Institute, China

C-P3 **Adaptive Ant Colony-Expectation-Maximization Hybrid Clustering for Clustered Single-Bit Failure Detection in DRAM Failbit Maps**
Jeong-eon Ahn, Hyung-gun Kim, Kwang-won Lee, Du-an Sun, Myung-Gyun Choi, Chang-soo Lee, Hee-il Hong
Samsung Electronics, South Korea

C-P4 **Integrated EOTPR and 3D XRM for non-destructive structural failure analysis in chip-scale packages**
Tianhan Liu[1], Yuanyang Liu[1], Zongbei Dai[1], Shaohua Yang[1], Chengcheng Chen[1], Wei Li[1], Liang Fang[1], Hongbo Qin[2], Liang Tan[3], Anyong Cai[4]
[1]*China Electronic Product Reliability and Environmental Testing Research Institute (CEPREI), China;* [2]*School of Mechanical and Electrical Engineering, Guilin University of Electronic Technology, China;* [3]*Guilin Power Capacitor Co., Ltd., China;* [4]*Guilin Zhiyuan Power Electronics Co., Ltd., China*

C-P5 **Localization of heating structures with a Scanning THermal AFM technique coupled with lock-in amplifier**
Guillaume Bascoul, Adrien Siguier
CNES Centre National d'Etudes Spatiales, France

C-P6 **Preparation-Induced Artefacts in PZT MLCCs: Implications for Microstructural Analysis**
Anina Anju Balaraman, Catriona Kenny, Ruth Houlihan
Tyndall National Institute, Ireland

Poster Session

E-P1 **Detection of Bond Wire Lift-Off Using Machine Learning on Switching Waveforms of Two Paralleled SiC-MOSFETs**

Kazune Idei[1], Jonas Müller[2], Hauke Lutzen[2], Nando Kaminski[2], Shin-Ichi Nishizawa[3], Wataru Saito[3]

[1]*Interdisciplinary Graduate School of Engineering Sciences (IGSES), Kyushu University, Japan;* [2]*Institute for Electrical Drives, Power Electronics and Devices (IALB), University of Bremen, Germany;* [3]*Research Institute for Applied Mechanics (RIAM), Kyushu University, Japan*

E-P2 **From Sample Preparation to Generative AI: A Comprehensive Characterization Workflow for Reliability Assessment of SAC305 Solder Interconnects**

Charlotte Cui[1], Roland Brunner[2], Fereshteh Falah Chamasemani[2], Pryia Paulachan[2], Rahulkumar Jagdishbhai Sinojiya[2], Jördis Rosc[2], Michael Tkadletz[3], Michael Reisinger[4], Peter Imrich[4], Walter Hartner[5], Werner Robl[5], Raphael Wilhelmer[2]

[1]*University of Leoben, Austria;* [2]*Materials Center Leoben Forschung GmbH, Austria;* [3]*Montanuniversität Leoben, Austria;* [4]*Kompetenzzentrum für Automobil- und Industrieelektronik GmbH, Austria;* [5]*Infineon Technologies AG, Germany*

E-P3 **Advanced Microstructural Characterization and Residual Stress Determination for Reliable Thin Films**

Rahulkumar J. Sinojiya[1], Charlotte Cui[2], Bernhard Sartory[1], Michael Tkadletz[3], Michael Reisinger[4], Peter Imrich[5], Raphael Wilhelmer[6], Johannes Zechner[7], Werner Robl[8], Roland Brunner[9]

[1]*Materials Center Leoben Forschung GmbH, Austria;* [2]*University of Leoben, Austria;* [3]*Technical University of Leoben, Austria;* [4]*KAI GmbH, Austria;* [5]*Kompetenzzentrum für Automobil- und Industrieelektronik GmbH, Austria;* [6]*Materials Center Leoben Forschungs GmbH, Austria;* [7]*Infineon Technologies Austria;* [8]*Infineon Technologies AG, Germany;* [9]*Material Center Leoben Forschung GmbH, Austria*

E-P4 **Aging performance of Al_2O_3–Ni substrates with a graded metal ceramic interface**

Romain Raisson[1], Sophie Guillemet-Fritsch[2], Thomas Herisson de Beauvoir[2], Aurélie Boisard[3], Cyrille Duchesne[4], Paul-Etienne Vidal[1]

[1]*Laboratoire Génie de Production - University of Technology of Tarbes, University of Toulouse, France;* [2]*CIRIMAT, INP CNRS, University of Toulouse, France;* [3]*Safran Tech, France;* [4]*DeepConcept, France*

E-P5 **Characterization of Temperature-Dependent Moisture Sorption in Electronic Laminates under HAST and Climatic Stress**

Saman Kohneh-Poushi[1], Rainer Pelzer[2], Florian Tschelisnig[3], Katrin Unger[1]

[1]*Electronic Sensors Unit, Silicon Austria Labs, Sandgasse 34, 8010 Graz, Austria;* [2]*Infineon Technologies Austria AG, Siemensstrasse 2, 9500 Villach, Austria;* [3]*R&D Electronic Solutions, AT & S Austria Technologie & Systemtechnik AG, Fabriksgasse 13, 8700 Leoben, Austria*

E-P6 **Stress and Orientation Dependent Surface Diffusion in Ruthenium Nano-Interconnects: A Kinetic Monte Carlo study**

Po-Han Chen[1], Hajdin Ceric[2], Asif Shah Altaf[3], Chih-Hsien Huang[1], Houman Zahedmanesh[4]

[1]*Department of Electrical Engineering, NCKU, Tainan, Taiwan;* [2]*Institute for Microelectronics, TU Wien, Vienna, Austria;* [3]*Department of Electronic Systems Engineering, IISc, Bangalore, India;* [4]*imec, Leuven, Belgium*

E-P7 **Lifetime Prediction and Improvement Mechanism of Palladium-coated Copper Wire under High Temperature Conditions**

Noritoshi Araki[1], Shinya Azuma[1], Motoki Eto[1], Takashi Yamada[1]

[1]*Nippon Micrometal Corporation, Japan*

E-P8 **Highly reliable Cu sintered heat dissipation spacer for double side cooling power modules**

Junha Baik, Byeongchan Kim, Ha-Young Yu, Dongjin Kim

Korea Institute of Industrial Technology, South Korea

E-P9 **Spatial Diagnosis of TIM Degradation Patterns in IGBT Modules via Transient Thermal Impedance and Structure Function Analysis**

Yi Liu[1], Yunhui Mei[1], Zhaoyuan Gu[2], Zhengyun Zhu[2], Mingyang Gao[2], Aoxue Xu[2], Jian Luo[2]

[1]*Tiangong University, China;* [2]*NARI Group Corporation (State Grid Electric Power Research Institute) NANJING NARI Power Semiconductor Company Ltd., China*

E-P10 **Role of intermetallic compounds in system-level thermo-mechanics of 3D stacked packaging**

Ha-Young Yu, Junha Baik, Dongjin Kim

Korea Institute of Industrial Technology, South Korea

Poster Session

E-P11 **Simplified Model of Degraded Thermal Resistance for Failure Prognostics in Power Modules**
Nobuyuki Shishido[1], Satoshi Nakano[2], Wataru Saito[2]
[1]*Kindai University, Japan;* [2]*Kyushu University, Japan*

F1-P1 **Determination of Polyimide Degradation by Electrochemical Setups and Analytical Characterization**
Florian Märzweiler[1], Valentin Jung[2], Maximilian Podsednik[1], Lars Varain[1], Günter Fafilek[2], Andreas Limbeck[2]
[1]*KAI GmbH, Austria;* [2]*TU Wien, Austria*

F1-P2 **Impact of the temperature coefficient of SiC MOSFETs on the power cycling lifetime**
Lukas Hein, Patrick Heimler, Josef Lutz, Thomas Basler
Chemnitz University of Technology, Germany

F1-P3 **Correlative examination of copper metallization layers using lab-based tomography and DFXM**
Laura Neumann[1], Michael Reisinger[2], Sebastian Moser[2], Marilyn Sarkis[3], Yaozhu Li[3], Carsten Detlefs[3], Sylvia Conzendorf[1], André Clausner[1], Cedric Corley-Wiciak[3]
[1]*Fraunhofer IKTS, Germany;* [2]*KAI, Austria;* [3]*ESRF, France*

F1-P4 **Avalanche Ruggedness of 600V Ultra-Fast Silicon Diodes under UIS and ESD Stress Conditions**
Giuseppe Capasso[1], Alice Inverno[1], Antonio Porricelli[1], Alessandro Borghese[2], Mansha Kansal[2], Michele Riccio[2], Giovanni Breglio[2], Andrea Irace[2], Luca Maresca[2]
[1]*University of Napoli - Federico II, Italy;* [2]*University of Naples - Federico II, Italy*

F2-P1 **Direct observation of the Vth hysteresis effect on the switching characteristics of SiC MOSFETs**
Chihiro Kawahara, Shiro Hino
Mitsubishi Electric Corporation, Japan

F2-P2 **Negative Activation Energy Under Dynamic Stress of 650 V E-mode GaN HEMTs**
Matteo Dell'Andrea[1], Mirco Boito[2], Manuel Fregolent[1], Riccardo Fraccaroli[1], Isabella Rossetto[1], Carlo De Santi[1], Martina Ruvolo[3], Marcello Giuffrida[3], Maria Eloisa Castagna[3], Ferdinando Iucolano[3], Gaudenzio Meneghesso[1], Enrico Zanoni[1], Matteo Meneghini[1]
[1]*University of Padova, Italy;* [2]*Formerly with University of Padova. Now with Infineon Technologies, Italy;* [3]*STMicroelectronics, Italy*

F2-P3 **Applicability of Gate Switching spectroscopy in 4H-SiC MOSFETs in the absence of holes by light-generated charge carriers**
Paul Stampfer[1], Christoph Leithold[2], Magdalena Weger[3], Emil Hartl[2], Gregor Pobegen[1]
[1]*KAI GmbH, Austria;* [2]*Silicon Austria Labs, Austria;* [3]*Infineon, Austria*

F2-P4 **Advanced Weibull Analysis of Dynamic H3TRB Reliability Tests in SiC Power Devices**
Michele Fiore[1], Mattia Musolino[2], Giuseppe Mauromicale[2], Gaetano Sequenzia[3], Alessandro Sitta[2]
[1]*STMicroelectronics, University of Catania, Italy;* [2]*STMicroelectronics, Italy;* [3]*University of Catania, Italy*

F2-P5 **Characterization of Spatially Resolved Dynamic RDS,on Effects in Lateral GaN HEMTs**
Boris Butej[1], Dominik Wieland[2], Christian Koller[2], Dionyz Pogany[3], Clemens Ostermaier[2]
[1]*Kompetenzzentrum Automobil- und Industrieelektronik GmbH, Austria;* [2]*Infineon Technologies Austria AG, Austria;* [3]*Institute of Solid State Electronics, TU Wien, Austria*

F2-P6 **Comprehensive Analysis of Worst-Case Dynamic RDS(ON) in Commercial p-GaN HEMTs: Influence of Bias and Temperature Under Soft-Switching**
Nasri Said[1], Maroun Alam[1], Valeria Rustichelli[1], Mohamed Matmat[1], Michel Perrel[2], David Tremouilles[3], Jean-Guy Tartarin[3], Fabio Coccetti[1]
[1]*IRT Saint Exupéry, France;* [2]*Thales Alenia Space, France;* [3]*LAAS-CNRS, France*

F2-P7 **Frequency-Domain Investigation of Interface Trap Relaxation in SiC Power MOSFETs**
Wongani Moyo, Guillaume Vine, Stephane Baffreau, Paul-Etienne Vidal
University of Technology Tarbes Occitanie Pyrénées, France

F2-P8 **Threshold Voltage Monitoring of SiC MOSFET during Power Cycling Test in a Multichip Setup**
Sarthak Swaroop Dash[1], Swapnil Sunil Roge[1], Christian Herold[1], Thomas Basler[2]
[1]*Chemnitz Power Labs GmbH, Germany;* [2]*TU Chemnitz, Germany*

F2-P9 **Avalanche and Short Circuit Ruggedness of SiC MOSFETs with Embedded Schottky Barrier Diodes**
Heaklig Ayala[1], Asad Mahmood[1], Jose Ortiz Gonzalez[1], Saeed Jahdi[2], Olayiwola Alatise[1]
[1]*University of Warwick, United Kingdom;* [2]*University of Bristol, United Kingdom*

Poster Session

F2-P10 **New insight on temperature dependent degradation of p-GaN Gate During positive gate bias stress through capacitance measurement**
Harold Razafimanjaka[1], David Trémouilles[2], Maroun Alam[3], Valeria Rustichelli[3], Abdelhakim Bourennane[2], Laurence Allirand[4]
[1]*LAAS-CNRS, France;* [2]*LAAS/CNRS, France;* [3]*IRT St-Exupery, France;* [4]*Schaeffler, France*

F2-P11 **Figure of Merit for Planar Power 4H-SiC MOSFET Under Short Circuit Operation**
Tien Anh Nguyen[1], Stéphane Lefebvre[1], Stéphane Azzopardi[2]
[1]*Laboratory SATIE - CNAM, France;* [2]*SAFRAN TECH, France*

F2-P12 **Effects of Deep P+ Structure on Single-Event Leakage Degradation in SiC Trench MOSFETs**
Yu Dong, Xiaoyu Yan, Yuzhu Liu, Chen Yang, Tiankun Liu, Jiande Liu, Pengfei Zhai, Jie Liu
Institute of modern physics, Chinese Academy of Sciences, China

F2-P13 **GaN HEMTs Dynamic Instabilities Caused by Gate Voltage Spikes via pGaN Potential Biasing**
Ludovic Roche[1], David Trémouilles[1], Emmanuel Marcault[2], Corinne Alonso[1]
[1]*LAAS-CNRS, University of Toulouse, UPS, Toulouse, France;* [2]*CEA, CEA Tech Occitanie, F-31670 Labège, France*

F2-P14 **TDRC-Based Electron Mobility Extraction in 4H-SiC MOSFETs Validated by Hall Measurements**
Marike Van Orden[1], Paul Stampfer[1], Alberta Bonanni[2], Rajdeep Adhikari[2], Bogdan Faina[2], Thomas Aichinger[3], Gregor Pobegen[1]
[1]*Kompetenzzentrum Automobil- und Industrieelektronik GmbH, Austria;* [2]*Institute of Semiconductor and Solid State Physics, JKU Linz, Austria;* [3]*Infineon Technologies Austria AG, Austria*

F3-P1 **Real Time Steady state Junction Temperature Estimation of DM9 Super Junction MOSFETs in HU3PAK**
Abhay Kumar, Sara Bourouga, Dario Catalano, Anselmo Gianluca Liberti
STMicroelectronics, Italy

F3-P2 **AI-Driven Framework for Frequency-Dependent ESL and ESR Estimation of DC-Link Capacitor in Inverter Applications**
Mohd Zubair Akhtar[1], Nima Tashakor[1], Gordon Elger[2], Silas Doerfer[1], Christian Sommer[1], Artjom Avakian[1]
[1]*Volkswagen AG, Germany;* [2]*Technische Hochschule Ingolstadt, Germany*

F3-P3	**Superimposed power cycling with fluid temperatures down to -30°C on SiC MOSFETs in double-sided cooled modules** Tobias Lentzsch, Sandro Richter, Josef Lutz, Thomas Basler *Chair of Power Electronics, Chemnitz University of Technology, Germany*
F3-P4	**Environment-Adaptive Air-Duct Blockage Diagnosis for PV Inverters: A Temperature-Stratified Random Forest Approach** Ming-Yao Ma, Ao-Jie Qin, Wei-Sheng Guo *Hefei University of Technology, China*
F3-P5	**Frequency-Domain Reflectometry for Early-Stage Degradation Detection** Minxi Chen[1], Ali Ibrahim[1], Zoubir Khatir[1] [1]*University Gustave Eiffel, SATIE Laboratory, France*
F3-P6	**A Reduced-Order Lumped Parameter Thermal Network for Internal Temperature Monitoring of Automotive DC-Link Capacitors** Yi Liu, Shengxiu Xu, Yunhui Mei *Tiangong University, China*
F3-P7	**Early Cooling Transient Analysis of Die-Attach Degradation in SiC MOSFET Modules** Zoubir Khatir[1], Richard Lallemand[2], Ali Ibrahim[2], Mounira Bouarroudj[2], Damien Ingrosso[1] [1]*Gustave Eiffel University, France;* [2]*University Gustave Eiffel, France*
H-P1	**Investigation of Electrical Properties of AlN thin films for Potential Application in RF-MEMS Capacitive Switch** Ioannis Kochylas[1], Jose Paolo Martins[2], John Theocharis[1], Doriane Jussey[2], Aymen Mahjoub[2], Etienne Eustache[2], Maria Giannouri[1], Afshin Ziaei[2], George Papaioannou[3] [1]*National and Kapodistrian University of Athens, Greece;* [2]*Thales Research and Technology, France;* [3]*University of Athens, Greece*

Poster Session

H-P2 **Reliability Study of a Monolithic Three-Axis MEMS Accelerometer with Asymmetric Three-Mass Structure for Life-Critical Cardiac Pacemaker Applications**
Shih Ching-Jui[1], Yeh Chia-Hung[2], Lin Yung-Chang[1], Huang Po-Wei[1]
[1]*Department of Mechanical and Automation Engineering, Taiwan;* [2]*Department of Industrial Engineering and Enterprise Information, Taiwan*

H-P3 **A Critique of Tunneling Current Models for CMUTs with Silicon Nitride Membranes**
Sazzadur Chowdhury, Chukwuebuka Okoro
University of Windsor, Canada

H-P4 **Evaluation of Breakage Prevention Method for 2D MEMS Mirrors by Logging the Frequency**
Marlene Schneider[1], Bernd Deutschmann[2], David Brunner[3]
[1]*Institute of Electronics, TU Graz / Infineon Technologies Austria AG, Austria;* [2]*Institute of Electronics, TU Graz, Austria;* [3]*Infineon Technologies Austria AG, Austria*

I-P1 **Long term effects of high TID on 45nm NAND**
Boubakr Rahmani[1], Alessandro Maria Romano[1], Stéphanie Anceau[1], Remi Granger[2], Luc Salvo[2]
[1]*CEA-Leti, 17 av. Des Martyrs 38054 Grenoble, France;* [2]*Université Grenoble Alpes, CNRS UMR5266, Grenoble INP, Laboratoire SIMaP, 38000, France*

I-P2 **Impact of Heavy-Ion Energy Straggling in SRAM Sensitive Regions on Single-Event Upset**
T. K. Liu, Q. Y. Chen, J. Liu, B. Ye, X. X. Lee, I. W. Yao, P. X. Zhao, J. D. Liu
Institute of Modern Physics, Chinese Academy of Sciences, Lanzhou, China

I-P3 **Towards a Laser-to-Beam SEU/SEL Methodology**
Ricardo Ascazubi[1], Bahar Ajdari[1]
[1]*Intel, United States*

J-P1 **Multi-strategy Burn-in Time Optimization Based on Weibull Distribution and Genetic Algorithm**
Zhiwei Zheng, Xuerong Ye, Cen Chen, Hao Chen, Guofu Zhai
Harbin Institute of Technology, China

J-P2 **Small-Sample SOH Forecasting and RUL Prediction for Electric Vehicle Batteries via Constrained Degradation Trajectory Augmentation**

Xinyi Zhang[1], Yixiao Jiang[1], Yunlong Li[2], Jing Luo[2], Chaojun Wang[2], Yuchen Song[1]

[1]*Harbin Institute of Technology, China;* [2]*Seres Auto Co.,Ltd, China*

J-P3 **Physics-Guided Spatiotemporal Temperature Estimation for Large-Format Lithium-Ion Batteries**

Qian Xu[1], Mingyao Ma[2], Liping Mo[2], Tingzhi Jiang[2]

[1]*Hefei University of Technology, China;* [2]*School of Electrical and Automation Engineering, Hefei University of Technology, Hefei, China*

Personal Notes

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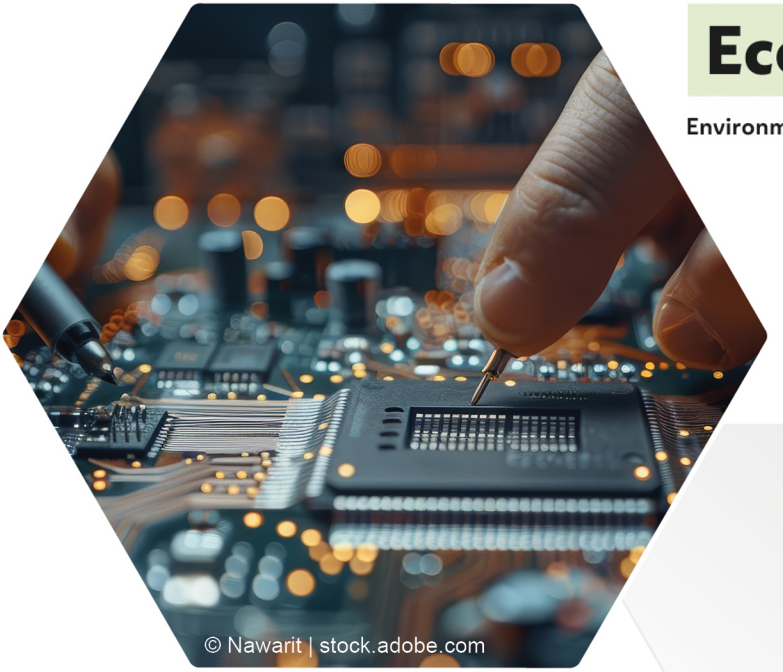
EcoEvent

Environment is VIP in Vienna



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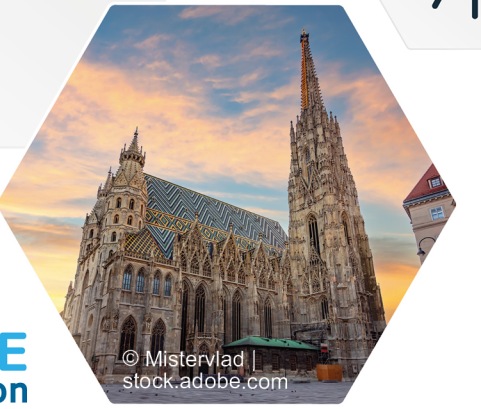

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PUBLISHER:

TU Wien
Institute for Microelectronics
Gusshausstrasse 27-29/E360
1040 Vienna
AUSTRIA

Issue: September 17, 2026

IEEE Austria Section

ISBN 978-3-200-11591-0